Datasheet

APM32F072xBT7

Arm® Cortex®-M0+ based 32-bit MCU (Automotive grade)

Version: V1.3

1 Product Characteristics

Core
- 32-bit Arm® Cortex®-M0+Core
- Up to 48MHz working frequency

On-Chip Memory
- Flash：128KB
- SRAM：16KB

Clock
- External 4~32MHz Crystal oscillator
- 32.768KHz oscillator with calibration
- Internal 8MHz RC oscillator
- Internal 14MHz RC oscillator
- Internal 48MHz self-correcting RC oscillator
- Internal 40KHz RC oscillator
- PLL supports 2~16 frequency doubling

Reset, Power Management
- Power-on/ Power-down reset (POR/PDR)
- Programmable voltage regulator
- Digital supply voltage: V_{DD}=2.0~3.6V
- Analog supply voltage: V_{DDA}=V_{DD}~3.6V
- Partial I/O supply voltage: V_{DDIO2}=1.65~3.6V
- Support external battery V_{BAT} to supply power to RTC and backup register: V_{BAT}=1.65~3.6V

Low Power Consumption Mode
- Sleep, halt and standby mode

Serial Wire Debugging (SWD)

I/O
- Up to 51 I/O
- All I/Os are mappable to external interrupt vectors
- 29 I/Os with 5V input tolerance，16 I/Os are powered by V_{DDIO2}

Communication Interface
- Two I2C interfaces (1Mbit/s), all of which support SMBus/PMBus and wake-up
- Four USART interfaces, all of which support master synchronous SPI and modem control, and two of them support ISO7816, LIN and IrDA interfaces, automatic baud rate detection and wake-up
- Two SPI interfaces (18Mbit/s), all supporting I2S interface multiplexing
- One CAN interface
- One full-speed USB2.0 interface, without external crystal oscillator, supporting BCD and LPM
- HDMI CEC

Analog Peripherals
- One 12-bit ADC, supporting 16 external channels, with conversion range of 0~3.6V, independent analog power supply: V_{DDA}=2.4~3.6V
- One dual, 12-bit DAC
- Two programmable analog comparators
- 18 capacitive sensing channels, which can be used for proximity, touch key, linear or rotary sensors

Timer
- One 16-bit advanced control timer which can provide 7 channels of PWM output, and supports dead zone generation and brake input functions
- One 32-bit and five 16-bit general timers, each timer has up to four independent channels for input capture/output comparison, PWM complementary, infrared control decoding or DAC control
- Two 16-bit basic timers
- One independent watchdog and one system window watchdog timer
- System tick timer

RTC
- Support calendar function
- Alarm and regular wake-up from halt/standby mode

7-Channel DMA Controller

CRC Calculation Unit

96-bit UID

Certification standards
- AEC-Q100-Rev-H September 11,2014

Contents

2 Product Information

See the following table for APM32F072xBT7 product functions and peripheral configuration.

Table 1 APM32F072xBT7 Series Chip Functions and Peripherals

Product		**APM32F072**	
Type		**CBT7**	**RBT7**
Package		**LQFP48**	**LQFP64**
Core and maximum working frequency		Arm® 32-bit Cortex®-M0+@48MHz	
Working voltage		2.0~3.6V	
Flash(KB)		128	
SRAM(KB)		16	
GPIOs		37	51
Communication interface	USART	4	
	SPI/I2S	2/2	
	I2C	2	
	USBD	1	
	CAN	1	
	CEC	1	
Timer	16-bit advanced	1	
	32-bit general	1	
	16-bit general	5	
	16-bit basic	2	
	System tick timer	1	
	Watchdog	2	
Real-time clock		1	
12-bit ADC	Unit	1	
	External channel	10	16
	Internal channel	3	
12-bit DAC	Unit	1	
	Channel	2	
Analog comparator		2	
Capacitance sensor channel		17	18
Working temperature		Ambient temperature: -40°C to 105°C Junction temperature: -40°C to 125°C	

3 Pin Information

3.1 Pin Distribution

Figure 1 Pin Distribution Diagram of APM32F072xBT7 Series LQFP48

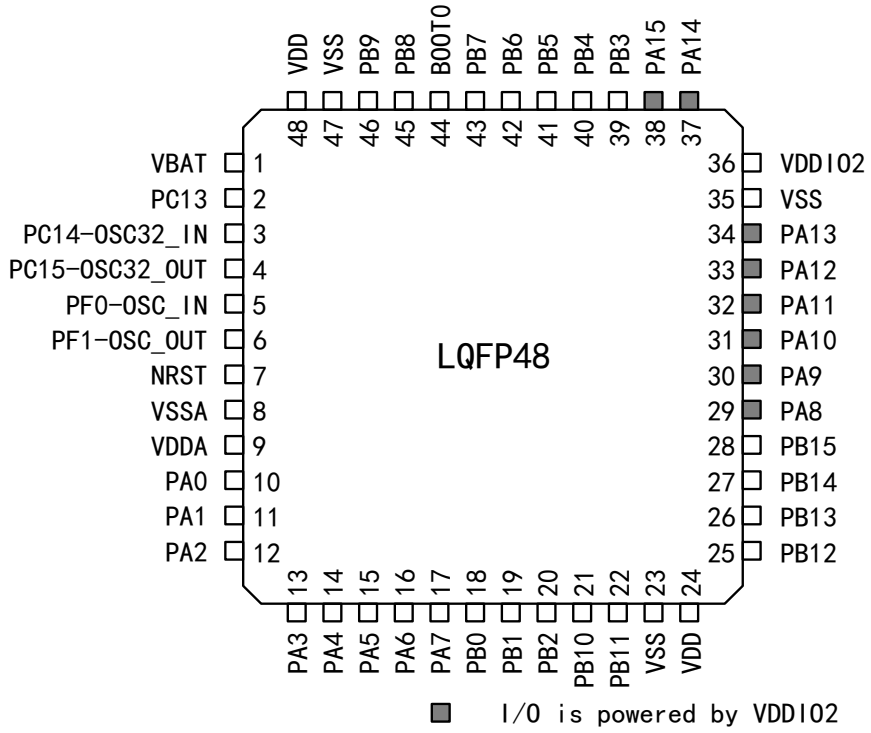
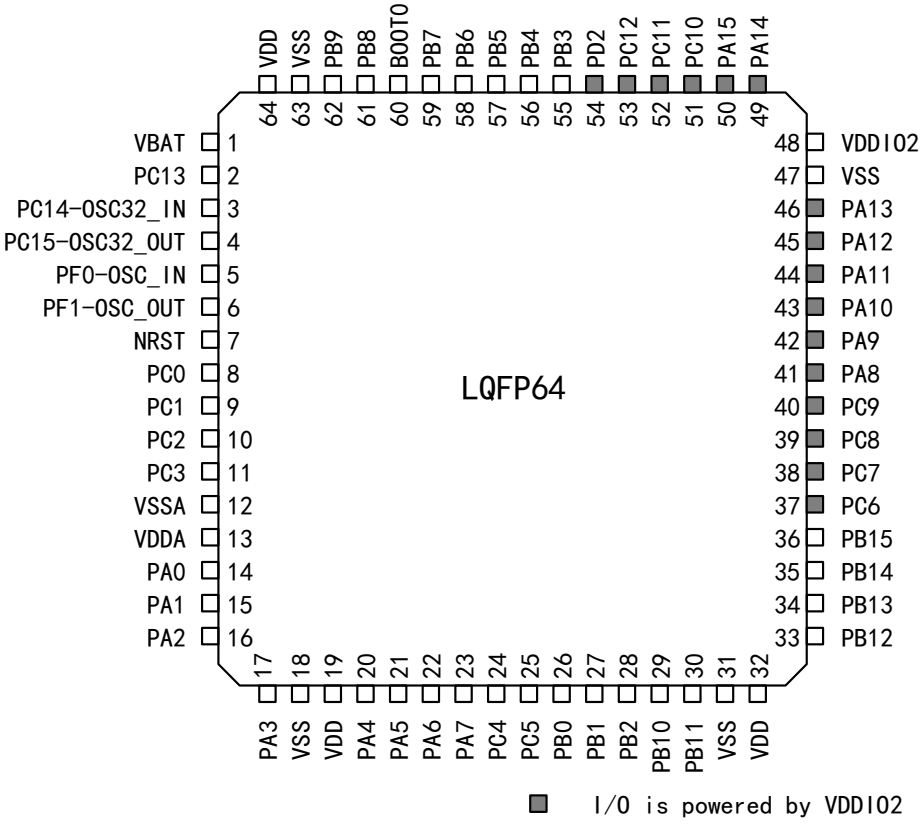


Figure 2 Pin Distribution Diagram of APM32F072xBT7 Series LQFP64



3.2 Pin Function Description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type		P	Power supply pin
		I	Input pins only
		I/O	I/O pins
I/O structure		5T	I/O with 5V tolerance
		5Tf	I/O, FM+ function with 5 V tolerance
		STDA	I/O with 3.3 V tolerance is directly connected to ADC
		STD	Standard 3.3VI/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with built-in weak pull-up resistor
Note		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Multiplexing function	The function selected by GPIOx_AFR register	
	Additional function	Functions directly selected/enabled through peripheral registers	

Table 3 APM32F072xBT7 Sort Description by Pin Serial Number

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	Pin ID	
					LQFP48	LQFP64
VBAT	—	—	P	—	1	1
PC13	—	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT	I/O	STD	2	2
PC14-OSC32_IN (PC14)	—	OSC32_IN	I/O	STD	3	3
PC15-OSC32_OUT (PC15)	—	OSC32_OUT	I/O	STD	4	4
PF0-OSC_IN (PF0)	CRS_SYNC	OSC_IN	I/O	5T	5	5
PF1-OSC_OUT (PF1)	—	OSC_OUT	I/O	5T	6	6
NRST	—	—	I/O	RST	7	7

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	Pin ID	
					LQFP48	LQFP64
PC0	EVENTOUT	ADC_IN10	I/O	STDA	-	8
PC1	EVENTOUT	ADC_IN11	I/O	STDA	-	9
PC2	SPI2_MISO, I2S2_MCK, EVENTOUT	ADC_IN12	I/O	STDA	-	10
PC3	SPI2_MOSI, I2S2_SD, EVENTOUT	ADC_IN13	I/O	STDA	-	11
VSSA	—	—	P	—	8	12
VDDA	—	—	P	—	9	13
PA0	USART2_CTS, TMR2_CH1_ETR, COMP1_OUT, TSC_G1_IO1, USART4_TX	RTC_TAMP2, WKUP1, ADC_IN0, COMP1_INM6	I/O	STDA	10	14
PA1	USART2_RTS, TMR2_CH2, TMR15_CH1N, TSC_G1_IO2, USART4_RX, EVENTOUT	ADC_IN1, COMP1_INP	I/O	STDA	11	15
PA2	USART2_TX, COMP2_OUT, TMR2_CH3, TMR15_CH1, TSC_G1_IO3	ADC_IN2, COMP2_INM6, WKUP4	I/O	STDA	12	16
PA3	USART2_RX, TMR2_CH4, TMR15_CH2, TSC_G1_IO4	ADC_IN3, COMP2_INP	I/O	STDA	13	17
VSS	—	—	P	—	-	18
VDD	—	—	P	—	-	19
PA4	SPI1_NSS, I2S1_WS, TMR14_CH1, TSC_G2_IO1, USART2_CK	COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT1	I/O	STDA	14	20

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	Pin ID	
					LQFP48	LQFP64
PA5	SPI1_SCK, I2S1_CK, CEC, TMR2_CH1_ETR, TSC_G2_IO2	COMP1_INM5, COMP2_INM5, ADC_IN5, DAC_OUT2	I/O	STDA	15	21
PA6	SPI1_MISO, I2S1_MCK, TMR3_CH1, TMR1_BKIN, TMR16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6	I/O	STDA	16	22
PA7	SPI1_MOSI, I2S1_SD, TMR3_CH2, TMR14_CH1, TMR1_CH1N, TMR17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7	I/O	STDA	17	23
PC4	EVENTOUT, USART3_TX	ADC_IN14	I/O	STDA	-	24
PC5	TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5	I/O	STDA	-	25
PB0	TMR3_CH3, TMR1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8	I/O	STDA	18	26
PB1	TMR3_CH4, USART3_RTS, TMR14_CH1, TMR1_CH3N, TSC_G3_IO3	ADC_IN9	I/O	STDA	19	27
PB2	TSC_G3_IO4	—	I/O	5T	20	28

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	Pin ID	
					LQFP48	LQFP64
PB10	SPI2_SCK, I2C2_SCL, USART3_TX, CEC, TSC_SYNC, TMR2_CH3	—	I/O	5T	21	29
PB11	USART3_RX, TMR2_CH4, EVENTOUT, TSC_G6_IO1, I2C2_SDA	—	I/O	5T	22	30
VSS	—	—	P	—	23	31
VDD	—	—	P	—	24	32
PB12	TMR1_BKIN, TMR15_BKIN, SPI2_NSS, I2S2_WS, USART3_CK, TSC_G6_IO2, EVENTOUT	—	I/O	5T	25	33
PB13	SPI2_SCK, I2S2_CK, I2C2_SCL, USART3_CTS, TMR1_CH1N, TSC_G6_IO3	—	I/O	5Tf	26	34
PB14	SPI2_MISO, I2S2_MCK, I2C2_SDA, USART3_RTS, TMR1_CH2N, TMR15_CH1, TSC_G6_IO4	—	I/O	5Tf	27	35
PB15	SPI2_MOSI, I2S2_SD, TMR1_CH3N, TMR15_CH1N, TMR15_CH2	WKUP7, RTC_REFIN	I/O	5T	28	36
PC6	TMR3_CH1	—	I/O	5T	-	37

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	Pin ID	
					LQFP48	LQFP64
PC7	TMR3_CH2	—	I/O	5T	-	38
PC8	TMR3_CH3	—	I/O	5T	-	39
PC9	TMR3_CH4	—	I/O	5T	-	40
PA8	USART1_CK, TMR1_CH1, EVENTOUT, MCO, CRS_SYNC	—	I/O	5T	29	41
PA9	USART1_TX, TMR1_CH2, TMR15_BKIN, TSC_G4_IO1	—	I/O	5T	30	42
PA10	USART1_RX, TMR1_CH3, TMR17_BKIN, TSC_G4_IO2	—	I/O	5T	31	43
PA11	CAN_RX, USART1_CTS, TMR1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT	USBD_DM	I/O	5T	32	44
PA12	CAN_TX, USART1_RTS, TMR1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT	USBD_DP	I/O	5T	33	45
PA13	IR_OUT, SWDIO, USBD_NOE	—	I/O	5T	34	46
VSS	—	—	P	—	35	47
VDDIO2	—	—	P	—	36	48
PA14	USART2_TX, SWCLK	—	I/O	5T	37	49

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	Pin ID	
					LQFP48	LQFP64
PA15	SPI1_NSS, I2S1_WS, USART2_RX, USART4_RTS, TMR2_CH1_ETR, EVENTOUT	—	I/O	5T	38	50
PC10	USART3_TX, USART4_TX	—	I/O	5T	-	51
PC11	USART3_RX, USART4_RX	—	I/O	5T	-	52
PC12	USART3_CK, USART4_CK	—	I/O	5T	-	53
PD2	USART3_RTS, TMR3_ETR	—	I/O	5T	-	54
PB3	SPI1_SCK, I2S1_CK, TMR2_CH2, TSC_G5_IO1, EVENTOUT	—	I/O	5T	39	55
PB4	SPI1_MISO, I2S1_MCK, TMR17_BKIN, TMR3_CH1, TSC_G5_IO2, EVENTOUT	—	I/O	5T	40	56
PB5	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TMR16_BKIN, TMR3_CH2	WKUP6	I/O	5T	41	57
PB6	I2C1_SCL, USART1_TX, TMR16_CH1N, TSC_G5_I03	—	I/O	5Tf	42	58

Name (Function after reset)	Multiplexing function	Additional function	Type	Structure	Pin ID	
					LQFP48	LQFP64
PB7	I2C1_SDA, USART1_RX, USART4_CTS, TMR17_CH1N, TSC_G5_IO4	—	I/O	5Tf	43	59
BOOT0	—	—	I	B	44	60
PB8	I2C1_SCL, CEC, TMR16_CH1, TSC_SYNC, CAN_RX	—	I/O	5Tf	45	61
PB9	SPI2_NSS, I2S2_WS, I2C1_SDA, IR_OUT, TMR17_CH1, EVENTOUT, CAN_TX	—	I/O	5Tf	46	62
VSS	—	—	P	—	47	63
VDD	—	—	P	—	48	64

Notes：

（1） PC13, PC14 and PC15 are powered by the power switch. The use of PC13 to PC15 of GPIO is limited in output mode since the switch only absorbs a limited current (3 mA):

① When the heavy load is 30pF, the speed should not exceed 2MHz.

② It is not used as a current source (for example, driving light emitting diodes).

（2） After reset, these pins are configured as SWDIO and SWCLK multiplexing functions, and the internal pull-up of SWDIO pin and the internal pull-down of SWCLK pin are activated.

（3） The gray part is powered by V_{DDIO2}.

3.3 GPIO Multiplexing Function Configuration

Table 4 GPIOA Multiplexing Function Configuration

Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	—	USART2_CTS	TMR2_CH1_ETR	TSC_G1_IO1	USART4_TX	—	—	COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TMR2_CH2	TSC_G1_IO2	USART4_RX	TMR15_CH1N	—	—
PA2	TMR15_CH1	USART2_TX	TMR2_CH3	TSC_G1_IO3	—	—	—	COMP2_OUT
PA3	TMR15_CH2	USART2_RX	TMR2_CH4	TSC_G1_IO4	—	—	—	—
PA4	SPI1_NSS,I2S1_WS	USART2_CK	—	TSC_G2_IO1	TMR14_CH1	—	—	—
PA5	SPI1_SCK,I2S1_CK	CEC	TMR2_CH1_ETR	TSC_G2_IO2	—	—	—	—
PA6	SPI1_MISO,I2S1_MCK	TMR3_CH1	TMR1_BKIN	TSC_G2_IO3	USART3_CTS	TMR16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI,I2S1_SD	TMR3_CH2	TMR1_CH1N	TSC_G2_IO4	TMR14_CH1	TMR17_CH1	EVENTOUT	COMP2_OUT
PA8	MCO	USART1_CK	TMR1_CH1	EVENTOUT	CRS_SYNC	—	—	—
PA9	TMR15_BKIN	USART1_TX	TMR1_CH2	TSC_G4_IO1	—	—	—	—
PA10	TMR17_BKIN	USART1_RX	TMR1_CH3	TSC_G4_IO2	—	—	—	—
PA11	EVENTOUT	USART1_CTS	TMR1_CH4	TSC_G4_IO3	CAN_RX	—	—	COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TMR1_ETR	TSC_G4_IO4	CAN_TX	—	—	COMP2_OUT
PA13	SWDIO	IR_OUT	USBD_NOE	—	—	—	—	—
PA14	SWCLK	USART2_TX	—	—	—	—	—	—
PA15	SPI1_NSS,I2S1_WS	USART2_RX	TMR2_CH1_ETR	EVENTOUT	USART4_RTS	—	—	—

Table 5 GPIOB Multiplexing Function Configuration

Name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TMR3_CH3	TMR1_CH2N	TSC_G3_IO2	USART3_CK	—
PB1	TMR14_CH1	TMR3_CH4	TMR1_CH3N	TSC_G3_IO3	USART3_RTS	—
PB2	—	—	—	TSC_G3_IO4	—	—
PB3	SPI1_SCK,I2S1_CK	EVENTOUT	TMR2_CH2	TSC_G5_IO1	—	—
PB4	SPI1_MISO,I2S1_MCK	TMR3_CH1	EVENTOUT	TSC_G5_IO2	—	TMR17_BKIN
PB5	SPI1_MOSI,I2S1_SD	TMR3_CH2	TMR16_BKIN	I2C1_SMBA	—	—
PB6	USART1_TX	I2C1_SCL	TMR16_CH1N	TSC_G5_IO3	—	—
PB7	USART1_RX	I2C1_SDA	TMR17_CH1N	TSC_G5_IO4	USART4_CTS	—
PB8	CEC	I2C1_SCL	TMR16_CH1	TSC_SYNC	CAN_RX	—
PB9	IR_OUT	I2C1_SDA	TMR17_CH1	EVENTOUT	CAN_TX	SPI2_NSS,I2S2_WS
PB10	CEC	I2C2_SCL	TMR2_CH3	TSC_SYNC	USART3_TX	SPI2_SCK,I2S2_CK
PB11	EVENTOUT	I2C2_SDA	TMR2_CH4	TSC_G6_IO1	USART3_RX	—
PB12	SPI2_NSS,I2S2_WS	EVENTOUT	TMR1_BKIN	TSC_G6_IO2	USART3_CK	TMR15_BKIN
PB13	SPI2_SCK,I2S2_CK	—	TMR1_CH1N	TSC_G6_IO3	USART3_CTS	I2C2_SCL
PB14	SPI2_MISO,2S2_MCK	TMR15_CH1	TMR1_CH2N	TSC_G6_IO4	USART3_RTS	I2C2_SDA
PB15	SPI2_MOSI,I2S2_SD	TMR15_CH2	TMR1_CH3N	TMR15_CH1N	—	—

Table 6 GPIOC Multiplexing Function Configuration

Name	AF0	AF1
PC0	EVENTOUT	—
PC1	EVENTOUT	—
PC2	EVENTOUT	SPI2_MISO,I2S2_MCK
PC3	EVENTOUT	SPI2_MOSI,I2S2_SD
PC4	EVENTOUT	USART3_TX
PC5	TSC_G3_IO1	USART3_RX
PC6	TMR3_CH1	—
PC7	TMR3_CH2	—
PC8	TMR3_CH3	—
PC9	TMR3_CH4	—
PC10	USART4_TX	USART3_TX
PC11	USART4_RX	USART3_RX
PC12	USART4_CK	USART3_CK
PC13	—	—
PC14	—	—
PC15	—	—

Table 7 GPIOD Multiplexing Function Configuration

Name	AF0	AF1
PD2	TMR3_ETR	USART3_RTS

Table 8 GPIOF Multiplexing Function Configuration

Name	AF
PF0	CRS_SYNC
PF1	—

4 Function Description

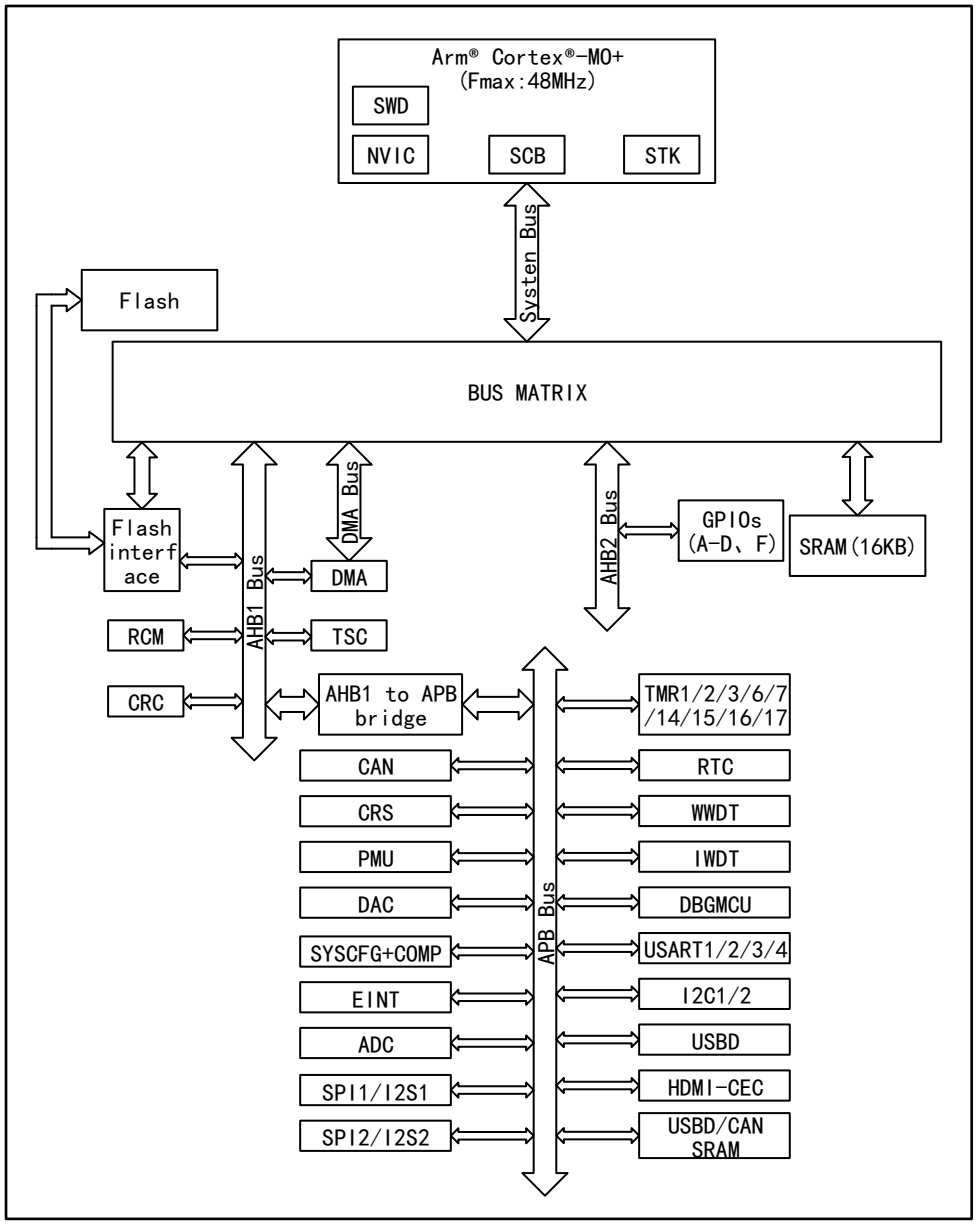
This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral characteristics of APM32F072xBT7 series products. For information about Arm® Cortex®-M0+core, please refer to the Arm® Cortex®-M0+technical reference sheet, which can be downloaded from Arm's website.

Currently, the APM32F072xBT7 model has passed the AEC-Q100-Rev-H September 11,2014 standard.

4.1 System Architecture

4.1.1 System Block Diagram

Figure 3 System Block Diagram



4.1.2 Storage Mapping

Table 9 APM32F072xBT7 Storage Mapping Table

Region	Start Address	Peripheral Name
Code	0x0000 0000	Code mapping area
Code	0x0002 0000	Reserve
Code	0x0800 0000	Main memory area
Code	0x0802 0000	Reserve
Code	0x1FFF C800	BootLoader
Code	0x1FFF F800	Option byte
Code	0x1FFF FC00	Reserve
SRAM	0x2000 0000	SRAM
—	0x2000 4000	Reserve
APB bus	0x4000 0000	TMR2
APB bus	0x4000 0400	TMR3
APB bus	0x4000 0800	Reserve
APB bus	0x4000 1000	TMR6
APB bus	0x4000 1400	TMR7
APB bus	0x4000 1800	Reserve
APB bus	0x4000 2000	TMR14
APB bus	0x4000 2400	Reserve
APB bus	0x4000 2800	RTC
APB bus	0x4000 2C00	WWDT
APB bus	0x4000 3000	IWDT
APB bus	0x4000 3400	Reserve
APB bus	0x4000 3800	SPI2/I2S2
APB bus	0x4000 3C00	Reserve
APB bus	0x4000 4400	USART2
APB bus	0x4000 4800	USART3
APB bus	0x4000 4C00	USART4
APB bus	0x4000 5000	Reserve
APB bus	0x4000 5400	I2C1
APB bus	0x4000 5800	I2C2
APB bus	0x4000 5C00	USBD
APB bus	0x4000 6000	USBD/CAN SRAM
APB bus	0x4000 6400	CAN
APB bus	0x4000 6800	Reserve
APB bus	0x4000 6C00	CRS
APB bus	0x4000 7000	PMU
APB bus	0x4000 7400	DAC
APB bus	0x4000 7800	HDMI-CEC

Region	Start Address	Peripheral Name
APB bus	0x4000 7C00	Reserve
APB bus	0x4000 8000	Reserve
APB bus	0x4001 0000	SYSCFG+COMP
APB bus	0x4001 0400	EINT
APB bus	0x4001 0800	Reserve
APB bus	0x4001 2400	ADC
APB bus	0x4001 2800	Reserve
APB bus	0x4001 2C00	TMR1
APB bus	0x4001 3000	SPI1/I2S1
APB bus	0x4001 3400	Reserve
APB bus	0x4001 3800	USART1
APB bus	0x4001 3C00	Reserve
APB bus	0x4001 4000	TMR15
APB bus	0x4001 4400	TMR16
APB bus	0x4001 4800	TMR17
APB bus	0x4001 4C00	Reserve
APB bus	0x4001 5800	DBGMCU
APB bus	0x4001 5C00	Reserve
—	0x4001 8000	Reserve
AHB1 bus	0x4002 0000	DMA
AHB1 bus	0x4002 0400	Reserve
AHB1 bus	0x4002 1000	RCM
AHB1 bus	0x4002 1400	Reserve
AHB1 bus	0x4002 2000	Flash Interface
AHB1 bus	0x4002 2400	Reserve
AHB1 bus	0x4002 3000	CRC
AHB1 bus	0x4002 3400	Reserve
AHB1 bus	0x4002 4000	TSC
—	0x4002 4400	Reserve
AHB2 bus	0x4800 0000	GPIOA
AHB2 bus	0x4800 0400	GPIOB
AHB2 bus	0x4800 0800	GPIOC
AHB2 bus	0x4800 0C00	GPIOD
AHB2 bus	0x4800 1000	Reserve
AHB2 bus	0x4800 1400	GPIOF
—	0x4800 1800	Reserve
Core	0xE000 E010	STK
Core	0xE000 E100	NVIC
Core	0xE000 ED00	SCB
—	0xE010 0000	Reserve

4.1.3 Startup Mode

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Boot from main memory
- Boot from BootLoader
- Boot from built-in SRAM

The user can use USART (PA14/PA15 or PA9/PA10), I2C(PB6/PB7) and USBDDFU interface to reprogram the user Flash if boot from BootLoader.

4.2 Core

The core of APM32F072xBT7 is Arm® Cortex®-M0+, which is the latest generation of embedded Arm core. Based on low development cost and power consumption characteristics of this platform, it can provide excellent calculation performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3 Interrupt Controller

4.3.1 Nested Vector Interrupt Controller (NVIC)

The APM32F072xBT7 product has a nested vector interrupt controller, and NVIC can handle up to 32 maskable interrupt channels (excluding 16 interrupt lines of Cortex®-M0+) and 4 priorities. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2 External Interrupt/ Event Controller (EINT)

The external interrupt/event controller has 32 edge detectors, each of which includes an edge detection circuit and an interrupt/event request generation circuit. Each detector can be configured as rising edge trigger, falling edge trigger and double edge trigger, and can also be shielded separately. Up to 51 GPIO can be connected to 16 external interrupt lines.

4.4 On-Chip Memory

User-modifiable memory includes main memory, SRAM, option byte and BootLoader. The BootLoader has been written at ex-works and cannot be modified.

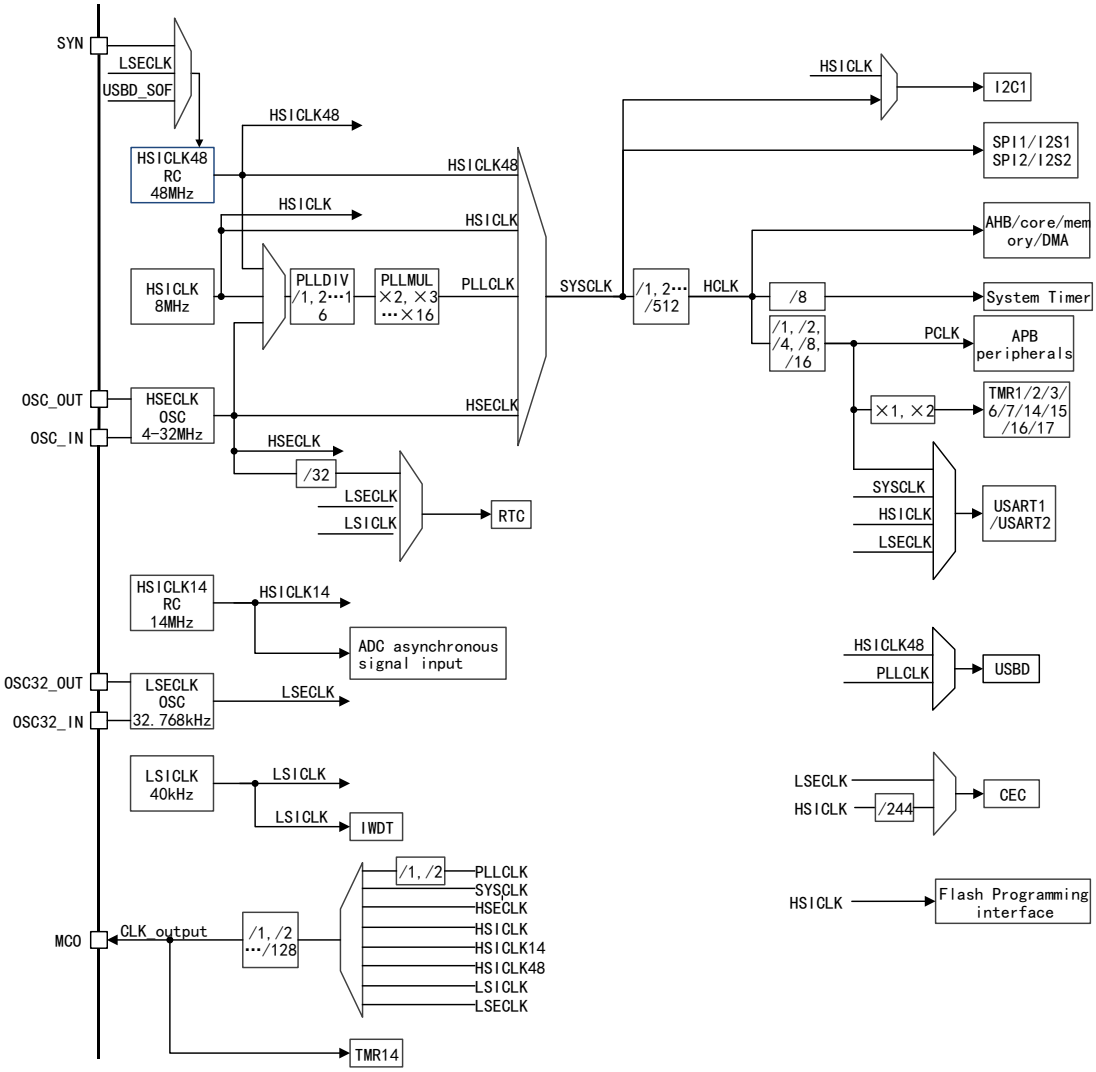
Table 10 Memory Description

Memory	Max bytes	Description
main memory	128KB	Store user's code and constant data
SRAM	16KB	—
Option byte	16Bytes	Three levels can be configured to protect part of the main memory or the whole main memory
BootLoader	12KB	—

4.5 Clock

See the following figure for clock tree of APM32F072xBT7:

Figure 4 APM32F072xBT7 Clock Tree



4.5.1 Clock Source

Clock sources of APM32F072xBT7 can be divided into high-speed clock and low-speed clock according to speed, with high-speed clocks including HSICLK48_CLK, HSICLK14_CLK, HSICLK_CLK and HSECLK, and low-speed clocks including LSECLK and LSICLK. On-chip/off-chip is divided into internal clock and external clock. The internal clocks are HSICLK48_CLK, HSICLK14_CLK, HSICLK_CLK and LSICLK, and the external clocks are HSECLK and LSECLK, among which HSICLK48_CLK, HSICLK14_CLK and HSICLK_CLK are calibrated at ex-works.

4.5.2 System Clock

The APM32F072xBT7 can select HSICLK48_CLK, HSICLK_CLK, PLL_CLK and HSECLK_CLK as system clocks. In which the clock source of HSICLK48_CLK is HSICLK48 and the clock source of HSICLK_CLK is HSICLK. One of HSICLK48_CLK, HSICLK and HSECLK can be selected as the clock source of PLL_CLK, and the required system clock can be obtained by configuring the frequency doubling coefficient and frequency division coefficient of PLL. Clock source of HSECLK_CLK is HSECLK. When the product is reset and started, HSICLK_CLK is selected as the system clock by default, and then the user can choose one of the above four clock sources as the system clock by himself.

4.5.3 Bus Clock

Clock source of AHB is SYC_CLK, clock source of APB is ABH_CLK, the required clock can be obtained by configuring frequency division coefficient, and the maximum value of AHB_CLK and APB_CLK is 48MHz.

4.6 Power Management

4.6.1 Power Supply Scheme

Table 11 Power Supply Scheme

Name	Voltage Range	Description
V_{DD}/V_{DDIO1}	2.0~3.6V	I/O (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V_{DD} pin.
V_{DDIO2}	1.65-3.6V	I/O is powered through V_{DDIO2} pin (see pin distribution diagram for specific IO).
V_{DDA}	V_{DD}~3.6V	The V_{DDA} supplies power to the ADC, reset module, RC oscillator and PLL, and the voltage level of V_{DDA} must always be greater than or equal to the voltage level of V_{DD}, which should be given priority.
V_{BAT}	1.65-3.6V	When V_{DD} is powered off, power can be supplied to RTC, external 32kHz oscillator and backup register through V_{BAT} pin.

Note: For more details on how to connect the power supply pins, see Figure 7 Power Supply Scheme

4.6.2 Voltage Regulator

Table 12 Working Mode of Regulator

Name	Description
Master mode (MR)	Used in running mode
Low power mode (LPR)	Used in halt mode
Power-down mode	Used in standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3 Power Supply Monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage regulator (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

4.7 Low Power Consumption Mode

APM32F072xBT7 supports three low power consumption modes: sleep mode, halt mode and standby mode. These three modes are different in power consumption, wake-up time and wake-up mode, so the low power consumption mode can be selected according to actual application requirements.

Table 13 Low Power Consumption Mode

Mode type	Description
Sleep mode	The CPU stops working, all peripherals are working, and interrupts/events can wake up the CPU.
halt mode	Under the condition that SRAM and register data are not lost, the halt mode can achieve the lowest power consumption; The clock of the internal 1.5V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be prohibited, and the voltage regulator can be configured in normal mode or low power consumption mode; Any external interrupt line can wake up MCU, including one of 16 external interrupt lines, PVD output, RTC, I2C1, USART1, USART2, analog comparator, USBD and CEC.
Standby mode	The mode power consumption is the lowest. Internal voltage regulator is turned off, all 1.5V power supply modules are powered off, HSECLK crystal resonator, HSICLK and PLL clocks are turned off, SRAM and register data disappear, RTC area and backup register contents remain, and standby circuit still works; The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

Note: RTC, IWDT and corresponding clocks still work normally in halt or standby mode.

4.8 GPIO

The working modes of GPIO can be configured as gengeral input, general output, multiplexing function and analog input/output. General input can be configured as floating input, pull-up input and pull-down input, while general output can be configured as push-pull output and open-drain output. Multiplexing function can be used for digital peripherals, while analog input/output can be used for analog peripherals and low power consumption mode. It can be configured with resistors that prohibit pull-up/pull-down. The speeds of 2MHz, 10MHz and 50MHz can be configured. The higher the speed, the greater the power consumption and noise.

4.9 Communication Interface

4.9.1 USART

Up to four universal synchronous/asynchronous transceivers are embedded in the chip, and the communication rate can support 6Mbit/s at most. All USART can be configured with baud rate, parity bit, stop bit and data bit length, and DMA controller can be used to support single-line half-duplex mode. The functional differences of 4 USART are shown in the following table.

Table 14 APM32F072xBT7 USART Functional Differences

USART Mode/Function	USART1/2	USART3/4
Hardware flow control of modem	√	√
Synchronization mode	√	√
Smart card mode	√	—
IrDASIR codec module	√	—
LIN mode	√	—
Dual clock domain and wake-up from halt mode	√	—
Receiver timeout interrupt	√	—
MODBUS communication	√	—
Automatic baud rate detection	√	—

Note: √ = support.

4.9.2 I2C

Built-in I2C1/2 can work in multi-master mode and slave mode. It supports 7-bit and 10-bit addressing modes, standard mode (up to 100kbit/s), fast mode (up to 400kbit/s) and ultra-fast mode (1Mbit/s). The DMA controller can be used.

In addition, I2C1 also provides hardware support for SMBUS2.0 and PMBUS1.1: ARP function, host notification protocol, hardware CRC(PEC) generation/verification, timeout verification and alarm protocol management.

See the following table for the differences between I2C1 and I2C2:

Table 15 APM32F072xBT7I2C 1/2 Functional Differences

I2C function	I2C1	I2C2
Independent clock	√	—
SM bus	√	—
Wake up from halt	√	—

Note:√=Support

4.9.3 SPI/I2S

Two built-in SPI support full-duplex and half-duplex communication in master mode and slave mode. The DMA controller can be used, which can be configured with 4~16 bits per frame and the highest communication rate is 18 mbit/s.

Two built-in I2S (multiplexed with SPI1 and SPI2, respectively) support half-duplex communication in master mode and slave mode, and support synchronous transmission, which can be configured with 16-bit, 24-bit and 32-bit data transmission of 16-bit or 32-bit resolution, and can be configured with audio sampling rate ranging from 8 kHz to 192 kHz.

4.9.4 HDMI-CEC

There is a built-in HDMI-CEC, the hardware supports consumer electronic control protocol, and there are two clock sources, HSICLK/255 and LSECLK. when LSECLK is selected as the clock source, HDMI_CEC is supported to wake up MCU in stop low power consumption mode.

4.9.5 CAN

A built-in CAN, conforming to CAN2.0A and CAN2.0B(active) specifications, the highest bit rate supporting 1Mbit/s, sending and receiving frame format supporting standard frame grid with 11-bit identifier and extended frame with 29-bit identifier, and allocating 256Bytes dedicated SRAM for sending and receiving data.

4.9.6 USBD

A built-in USBD, in line with full-speed USBD device 2.0 standard (12Mbit/s), supporting battery charging specification version 1.2, built-in USBD_PHY, configurable USBD_DP pull-up, eliminating external pull-up resistance. A dedicated SRAM data buffer of 1024Bytes is allocated (the last 256Bytes are shared with CAN), and HSICLK48_CLK and PLL_CLK can be selected as clock sources to generate 48MHz clock.

4.10 Analog Peripherals

4.10.1 ADC

Two built-in 12-bit ADCs, up to 16 external channels and 3 internal channels, which measure the temperature sensor voltage, reference voltage and V_{BAT} voltage respectively. It can be configured with the resolution, the sampling time is programmable, and it support self-calibration. The startup mode supports software trigger and hardware trigger. The conversion mode supports single conversion, continuous conversion and intermittent conversion, and the conversion channel selection supports single channel conversion and scanning conversion of a certain sequence of channels. It supports analog watchdog and DMA.

4.10.2 Temperature Sensor

A temperature sensor (TSensor) is built in, which is internally connected with ADC_IN16 channel. The voltage generated by the sensor changes linearly with temperature, and the converted voltage value can be obtained by ADC and converted into temperature.

The temperature sensor is calibrated at ex-works to obtain accurate values. The calibrated values are stored in a certain area of the memory, which is read-only, as shown in the following table. Uncalibrated temperature sensors are only used to detect temperature changes.

Table 16 Calibration Value of Temperature Sensor

Calibration Value Name	Description	Memory Address
TSensor_CAL1	Original data collected at V_{DDA}=3.3V(±10mV) under 25℃ (±5℃) by TSensor ADC	0x1FFF F7B8 - 0x1FFF F7B9

4.10.3 Calibration of Internal Reference Voltage (V_{REFINT})

Built-in reference voltage V_{REFINT}, internally connected to ADC_IN17 channel, which can be obtained through ADC; V_{REFINT} provides stable (band gap) voltage output for ADC and comparator. Calibrate at the ex-works and store the calibration value in the read-only area of the memory to improve the accuracy of the reference voltage.

Table 17 Calibration Value of Internal Reference Voltage

Calibration Value Name	Description	Memory Address
VREFINT_CAL	Original data collected at V_{DDA}=3.3V(±10mV) under 25℃ (±5℃)	0x1FFF F7BA - 0x1FFF F7BB

4.10.4 V_{BAT} Monitor

The built-in V_{BAT} monitor is internally connected to a 2-divider bridge, and V_{BAT}/2 is connected to ADC_IN18 channel, which can be obtained through ADC.

4.10.5 DAC

A built-in 12-bit DAC, it is 2 channels for output, which can be configured in 8-bit and 12-bit modes, and the DMA function is supported. The waveform generation supports noise wave and triangle wave. The conversion mode supports independent or simultaneous conversion and the trigger mode supports external signal trigger and internal timer update trigger.

4.10.6 Comparator

Two built-in fast rail-to-rail comparators, the internal/external reference voltage, hysteresis, speed and support are programmable, and the output polarity support is configurable. The reference voltage can be selected from external I/O, DAC output pin, internal reference voltage (VREFINT), and 1/4 or 1/2 or 3/4 of the internal reference voltage, which can generate interrupts, and support MCU entering sleep and stop modes by external interrupts.

4.10.7 Touch sensing controller

Built-in touch sensing controller can detect the change of capacitance, which can be applied to touch keys. When a finger touches a key, capacitance will be introduced, which will cause the capacitance change, so as to judge whether there is an eye-catching key. The touch sensing is compatible with slider, touch key, linear and rotary.

There are 24 GPIOs support capacitance sensor function, which are divided into 8 groups. In practical application, each sampling capacitor occupies one GPIO port, so there are 18 capacitance sensor channels are supported. See the table below for specific pin distribution.

Table 18 Applicable Pin Distribution of Touch Sensors

Group Number	Capacitance Sensor Signal Name	Pin Name
G1	TSC_G1_IO1	PA0
G1	TSC_G1_IO2	PA1
G1	TSC_G1_IO3	PA2
G1	TSC_G1_IO4	PA3
—		
G2	TSC_G2_IO1	PA4
G2	TSC_G2_IO2	PA5
G2	TSC_G2_IO3	PA6
G2	TSC_G2_IO4	PA7
—		
G3	TSC_G3_IO1	PC5
G3	TSC_G3_IO2	PB0

Group Number	Capacitance Sensor Signal Name	Pin Name
G3	TSC_G3_IO3	PB1
G3	TSC_G3_IO4	PB2
—		
G4	TSC_G4_IO1	PA9
G4	TSC_G4_IO2	PA10
G4	TSC_G4_IO3	PA11
G4	TSC_G4_IO4	PA12
—		
G5	TSC_G5_IO1	PB3
G5	TSC_G5_IO2	PB4
G5	TSC_G4_IO3	PB6
G5	TSC_G4_IO4	PB7
—		
G6	TSC_G6_IO1	PB11
G6	TSC_G6_IO2	PB12
G6	TSC_G6_IO3	PB13
G6	TSC_G6_IO4	PB14

Table 19 Number of Touch Sensor Channels Supported by Each Model in Practical Application

Group Number	Number of Channels for Each Group of Capacitance Sensors	
	APM32F072RBT7	APM32F072CBT7
G1	3	3
G2	3	3
G3	3	2
G4	3	3
G5	3	3
G6	3	3
Total Number of Capacitance Sensor Channels	18	17

4.11 Timer

A built-in 16-bit advanced timer TMR1, a 32-bit general timer TMR2, five 16-bit general timers TMR3/14/15/16/17, two basic timers TMR6/7, an independent watchdog timer, a window watchdog timer and a system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is a peripheral of the core, which has the function of automatic reloading. When the counter is 0, it can generate a masked system interrupt, which can be used for real-time operating system and general delay.

The characteristics are compared as follows:

Table 20 Advanced Timers

Projects	Description
Name	TMR1
Pin characteristics	A total of 9 pins: 1 external trigger signal input pin, 1 brake input signal pin, 3 pairs of complementary channel pins, 1 channel (non-complementary channel) pin
Counter resolution	16 bits
DMA function	Support
Complementary PWM output function of dead-time insertion	Support

Table 21 General Timer

Projects	描述					
Name	TMR2	TMR3	TMR14	TMR15	TMR16	TMR17
Pin characteristics	A total of 5 pins: 1 external trigger signal input pin, 4 channels (non-complementary channels) pins		1 channel pin	A total of 4 pins: 1 brake input signal pin, 1 pair of complementary channel pins, 1 channel (non-complementary channel) pin	A total of 3 pins: 1 brake input signal pin, 1 pair of complementary channel pins	
Counter resolution	32 bits	16 bits	16 bits	16 bits	16 bits	
DMA function	Support	Support	Non-support	Support	Support	
Complementary PWM output function of dead zone insertion	Non-support	Non-support	Non-support	Support		

Table 22 Basic Timers

Projects	描述
Name	TMR6/7
Pin characteristics	No pins
Counter resolution	16 bits
DMA function	Support
Complementary PWM output function of dead zone insertion	Non-support

Table 23 Independent Watchdog and Window Watchdog Timers

Name	Counter resolution	Counter type	Prescaler coefficient	Clock source	Generate signal
Independent watchdog（IWDT）	12 bits	down	Any integer between 1 and 256	LSICLK	Reset signal
Window watchdog（WWDT）	7 bits	down	-	Clock divided by APB1	Reset signal or interrupt signal

Table 24 System Tick Timer

Timer type	describe
Pin characteristics	No pins
Counter resolution	24 bits
Clock source	HCLK or HCLK/8
DMA function	Non-support
Complementary PWM output function of dead zone insertion	Non-support

4.12 Real-Time Clock（RTC）

A built-in RTC with LSECLK signal input pins (OSC32_IN, OSC32_OUT), three TAMP input signal detection pins (RTC_TAMP1/2/3), one reference clock input signal (RTC_REFIN), one output timestamp event output pin (RTC_TS), and one signal output pin RTC_OUT (It can be configured as calibration signal output or alarm clock signal output).

The external crystal oscillator, resonator or oscillator, LSICLK and HSECLK/32 with external frequency of 32.768kHz can be selected as the clock source.

With calendar function, it can display sub-seconds, seconds, minutes, hours (12 or 24 hours format), weeks, dates, months and years. It supports alarm clock function, output alarm clock signal for external use, and wake up from low power consumption mode. It can receive signals to wake up from low power consumption mode. In terms of accuracy, it supports daylight saving time compensation, month angel compensation and leap year days compensation. In terms of accuracy, the error caused by crystal oscillator can be repaired by RTC digital calibration function, and the accuracy of calendar can be improved by using a more accurate second source clock (50 or 60Hz).

4.13 CRC calculation unit

A CRC (cyclic redundancy check) calculation unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

4.14 DMA

A built-in DMA supports seven DMA channels, each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI1/2, USART1/2/3/4, I2C1/2, TMR1, TMR2, TMR3, TMR6, TMR7, TMR15, TMR16 and TMR17. Four levels of DMA channel priority can be configured, and data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" can be supported (memory includes Flash and SRAM).

5 Electrical Characteristics

5.1 Test Conditions of Electrical Characteristics

All voltage parameters (unless otherwise specified) refer to V_{SS}.

5.1.1 Maximum and Minimum Values

Unless otherwise specified, all products are tested on the production line at TA=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data obtained through comprehensive evaluation, design simulation or process characteristics are not tested on the production line. On the basis of comprehensive evaluation, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values after passing the sample test.

5.1.2 Typical values

Unless otherwise specified, typical data are measured based on T_A=25℃,

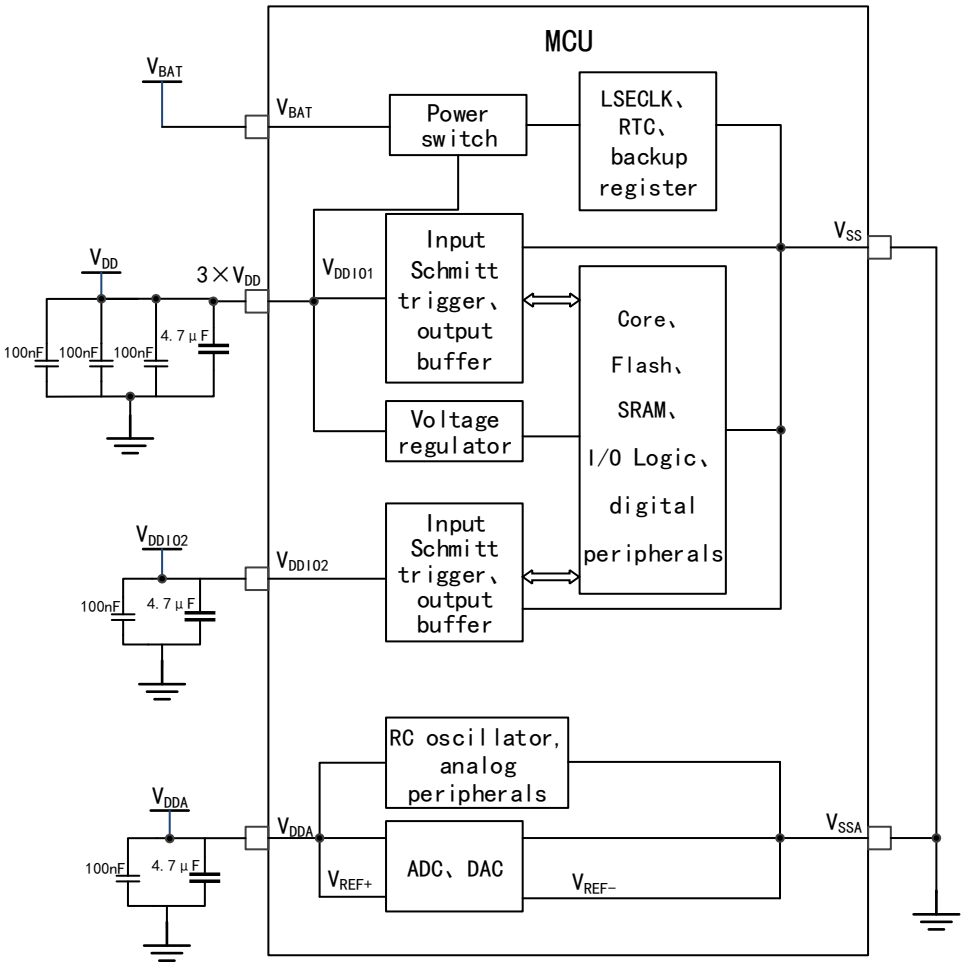
V_{DD}=V_{DDIO2}=V_{DDA}=3.3V. these data are only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves will not be tested on the production line, and will only be used for design guidance.

5.1.4 Power Supply Scheme

Figure 5 Power Supply Scheme



5.1.5 Load Capacitance

Figure 6 Load Conditions when Measuring Pin Parameters

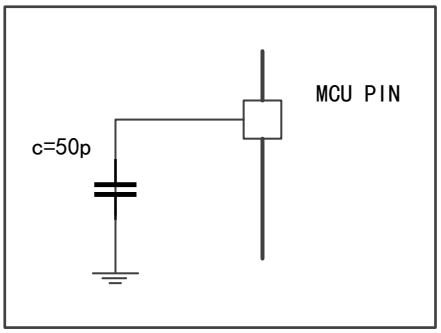


Figure 7 Pin Input Voltage Measurement Scheme

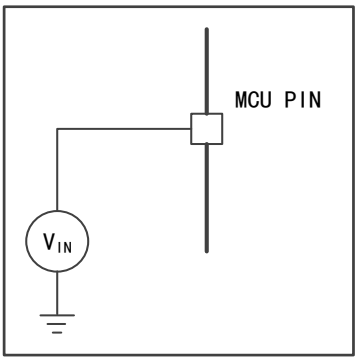
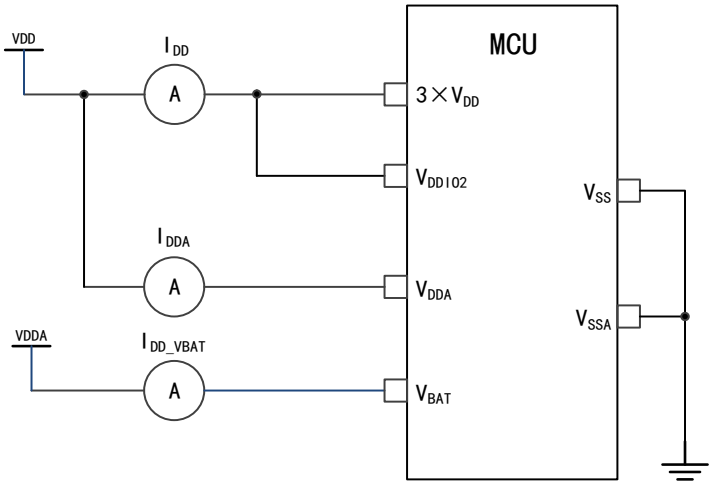


Figure 8 Power Consumption Measurement Scheme



5.2 Testing under General Working Conditions

Table 25 General Working Conditions

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz
f_{PCLK}	Internal APB clock frequency	-	-	48	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDIO2}	IO supply voltage	Only V_{DD} exists to supply power	1.65	3.6	V
V_{DDA}	Analog operating voltage (when neither ADC nor DAC is used)	V_{DDA} must not be less than V_{DD}	V_{DD}	3.6	V
	Analog operating voltage (when ADC and DAC is used)		2.4	3.6	
V_{BAT}	Backup area working voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	STD and RST I/O	-0.3	V_{DDIOX}+0.3	V
		STDA I/O	-0.3	V_{DDA}+0.3	
		5T and 5Tf I/O	-0.3	5.5	

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
		Boot0	0	5.5	

5.3 Absolute Maximum Rating

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1 Maximum Temperature Characteristics

Table 26 Temperature Characteristics

Symbol	Description	Numerical value	Unit
T_{STG}	Storage temperature range	–65~+150	℃
T_J	Maximum junction temperature	150	℃

5.3.2 Maximum Rated Voltage Characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 27 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD}-V_{SS}	External main supply voltage (V_{DD})	-0.3	4.0	V
V_{DDA}-V_{SSA}	External analog supply voltage（V_{DDA}）	-0.3	4.0	
V_{DDIO2}-V_{SS}	External I/O supply voltage	-0.3	4.0	
V_{BAT}-V_{SS}	External backup power supply voltage	-0.3	4.0	
$\lvert V_{DD}-V_{DDA} \rvert$	Allowable voltage difference of V_{DD}>V_{DDA}	-	0.3	
V_{IN}	Input voltage on 5T and 5Tf pins	V_{SS}-0.3	V_{DDIOX}+4.0	
	Input voltage on STDA pin	V_{SS}-0.3	4.0	
	Boot0	0	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS}-0.3	4.0	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins	-	50	mV
$\lvert V_{SSx}-V_{SS} \rvert$	Voltage difference between different grounding pins	-	50	

5.3.3 Maximum Rated Current Characteristics

Table 28 Maximum Rated Current Characteristics

Symbol	Description	Maximum value	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	-120	

Symbol	Description	Maximum value	Unit
$I_{DD\ (PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{SS\ (PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	-100	
$I_{IO\ (PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO\ (PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
	Total output current sourced by sum of all I/Os supplied by V_{DDIO2}	-40	
$II_{INJ(PIN)}$ (3)	Injected current on B, 5T and 5Tf pins	-5/+0 (4)	
	Injected current on STD and RST pin	±5	
	Injected current on STDA pins(5)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	±25	

（1） All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

（2） This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.

（3） A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.

（4） Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

（5） On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device.

（6） When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3.4 ESD Characteristics

Table 29 ESD Characteristics

Symbol	Parameter	Condition	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (manikin)	T_A=+25℃, conforming to AEC-Q100-002-REV –E(August 20, 2003)	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A=+25℃, conforming to AEC-Q100-002-REV –E(August 20, 2003)	750	

Note: It is tested by a third-party testing organization instead of in production.

5.3.5 Static Latch-up

Table 30 Static Latch-up

Symbol	Parameter	Condition	Type
LU	Room Temperature Latch-up	Room temperature(+25℃), ±200mA/1.5 VccMax, conforming to AEC-Q100-004-REV-D(August 7, 2012)	CLASS Ⅰ A
	High Temperature Latch-up	High temperature(+105℃), ±200mA/1.5 VccMax, conforming to AEC-Q100-004-REV-D(August 7, 2012)	CLASS Ⅱ A

Note: It is tested by a third-party testing organization instead of in production.

5.4 On-Chip Memory

5.4.1 Flash Characteristics

Table 31 Flash Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{prog}	16 bit programming time	T_A=-40~105℃, V_{DD}=2.0~3.6V	-	36	-	μs
t_{ERASE}	Page (2KB) erase time	T_A=-40~105℃, V_{DD}=2.0~3.6V	-	3	-	ms
t_{ME}	Whole erase time	T_A=25℃, V_{DD}=3.3V	-	6.4	-	ms
V_{prog}	Programming voltage	T_A=-40~105℃	2	-	3.6	V
N_{RW}	Erase cycle	T_A=25℃	-	10K	-	cycles

Note: It is tested in comprehensive evaluation instead of in production.

5.5 Clock System

5.5.1 Characteristics of External Clock Source

High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 32 Characteristics of HSECLK 4 ~ 32 MHz Oscillator

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	200	-	kΩ
I_{DD}	HSECLK current consumption	V_{DD}=3.3V, C_L=10pF@8MHz	-	0.5	-	mA
$t_{SU(HSECLK)}$	Startup time	V_{DD} is stable	-	2	-	ms

Note: It is tested in comprehensive evaluation instead of in production.

Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please

consult the corresponding manufacturer.

Table 33 LSECLK oscillator characteristics (fLSECLK=32.768KHz)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
I_{DD}	LSECLK current consumption	High driving ability	-	-	1.6	μA
$t_{SU(LSECLK)}$(1)	Startup time	V_{DDIOx} is stable	-	2	-	s

Note: It is tested in comprehensive evaluation instead of in production.

（1） $t_{SU(LSECLK)}$ is the starting time, which is measured from the software enabling LSECLK until the stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary from crystal manufacturer to crystal manufacturer.

5.5.2 Characteristics of Internal Clock Source

High speed internal (HSICLK)RC oscillator

Table 34 HSICLK Oscillator Characteristics

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
f_{HSICLK}	Frequency	-		-	8	-	MHz
ACC_{HSICLK}	Accuracy of HSICLK oscillat	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~105℃	-2.8	-	3.8	%
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V T_A=-40~105℃		1	-	2	μs
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-		-	80	100	μA

Note: Except for (1) calibration in production, other data are obtained in comprehensive evaluation instead of in production.

Table 35 HSICLK14 Oscillator Characteristics

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
$f_{HSICLK14}$	Frequency	-		-	14	-	MHz
$ACC_{HSICLK14}$	Accuracy of HSICLK14 oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~105℃	-4.2	-	5.1	%
$t_{SU(HSICLK14)}$	Startup time of HSICLK14 oscillator	V_{DD}=3.3V T_A=-40~105℃		1	-	2	μs
$I_{DDA(HSICLK14)}$	Power consumption of HSICLK14 oscillator	-		-	100	150	μA

Note: Except for (1) calibration in production, other data are obtained in comprehensive evaluation instead of in production.

Table 36 HSICLK48 Oscillator Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$f_{HSICLK48}$	Frequency	-	-	48	-	MHz

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
$Acc_{HSICLK48}$	Accuracy of HSICLK48 oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~105℃	-4.9	-	4.7	%
$t_{SU(HSICLK48)}$	Startup time of HSICLK48 oscillator	V_{DD}=3.3V，T_A=-40~105℃		-	-	6	μs
$I_{DDA(HSICLK48)}$	Power consumption of HSICLK48 oscillator	-		-	312	350	μA

Note: Except for (1) calibration in production, other data are obtained in comprehensive evaluation instead of in production.

Low speed internal (LSICLK)RC oscillator

Table 37 LSICLK Oscillator Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value
f_{LSICLK}	Frequency（V_{DD}=2-3.6V，T_A=-40~105℃）	30	40	50	KHz
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator（V_{DD}=3.3V，T_A=-40~105℃）	-	-	85	μs
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	0.75	1.2	μA

Note: It is tested in comprehensive evaluation instead of in production.

5.5.3 PLL Characteristics

Table 38 PLL Characteristics

Symbol	Parameter	Numerical value			Unit
		Minimum value	Typical value	Maximum value	
f_{PLL_IN}	PLL input clock	1	8.0	24	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock (V_{DD}=3.3V，T_A=-40~105℃）	-	48	-	MHz
t_{LOCK}	PLL phase locking time	-	-	200	μs

Note: It is tested in comprehensive evaluation instead of in production.

5.6 Power Management

5.6.1 Power-on/power-down characteristics

Table 39 Power-on/power-down Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{VDD}	V_{DD} rise time rate	-	1	-	310000	μs/V
	V_{DD} fall time rate		1	-	310000	

5.6.2 Characteristic test of embedded reset and power control module

Table 40 Embedded Reset and Power Control Module Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{POR/PDR}$(1)	Power-on/power-down reset threshold	Falling edge	1.87	1.90	1.94	V
		Rising edge	1.91	1.94	1.97	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$	Reset duration	-	0.80	1.14	1.89	ms

Note: It is tested in comprehensive evaluation instead of in production.

（1）PDR detector monitors V_{DD} and V_{DDA} (if enabled in option byte), POR detector monitors V_{DD} only.

Table 41 Programmable Voltage Detector Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Level selection of programmable voltage detector	PLS[2:0]=000 (rising edge)	2.16	2.20	2.24	V
		PLS[2:0]=000 (falling edge)	2.06	2.10	2.14	V
		PLS[2:0]=001 (rising edge)	2.25	2.30	2.36	V
		PLS[2:0]=001 (falling edge)	2.14	2.20	2.25	V
		PLS[2:0]=010 (rising edge)	2.37	2.40	2.44	V
		PLS[2:0]=010 (falling edge)	2.26	2.30	2.33	V
		PLS[2:0]=011 (rising edge)	2.46	2.50	2.54	V
		PLS[2:0]=011 (falling edge)	2.36	2.40	2.43	V
		PLS[2:0]=100 (rising edge)	2.57	2.60	2.62	V
		PLS[2:0]=100 (falling edge)	2.46	2.50	2.51	V
		PLS[2:0]=101 (rising edge)	2.61	2.70	2.79	V
		PLS[2:0]=101 (falling edge)	2.52	2.60	2.68	V
		PLS[2:0]=110 (rising edge)	2.74	2.80	2.87	V
		PLS[2:0]=110 (falling edge)	2.62	2.70	2.76	V
		PLS[2:0]=111 (rising edge)	2.81	2.90	2.99	V
		PLS[2:0]=111 (falling edge)	2.71	2.80	2.89	V
$V_{PVDhyst}$	PVD hysteresis	-	-	100	-	mV

Note: It is tested in comprehensive evaluation instead of in production.

5.7 Power Consumption

5.7.1 Power consumption test environment

（1） Test under the conditions of Coremark, KeilV5 compiling environment and L3 compiling optimization level.

（2） All I/O pins are configured as analog inputs, which are connected to V_{DD} or V_{SS} (non-load) at a static level.

（3） Unless otherwise specified, all peripherals are turned off.

（4） The relationship between the setting of flash waiting period and f_{HCLK}:

0~24MHz: 0 waiting periods,

24~48MHz: 1 waiting periods.

（5） Instruction prefetch function is enabled (Note: this bit must be set before clock setting and bus frequency division).

（6） When the peripheral is turned on: $f_{PCLK}=f_{HCLK}$.

5.7.2 Running mode

Table 42 The program is executed in Flash, and the power consumption in running mode

Parameter	Condition	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃, V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA）	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in running mode	HSECLK bypass(2), enabling all peripherals	48MHz	102.28	12.17	118.82	14.11
		32MHz	71.61	8.32	86.71	8.98
		24MHz	58.13	6.59	73.20	7.29
		8MHz	3.48	2.42	13.04	3.00
		1MHz	3.46	0.60	12.77	0.82
	HSECLK bypass(2), turn off all peripherals	48MHz	102.27	7.46	118.94	7.91
		32MHz	71.58	5.10	86.79	5.80
		24MHz	58.20	4.20	73.02	4.63
		8MHz	3.48	1.65	12.92	2.10
		1MHz	3.47	0.51	12.79	0.68
	HSICLK48, enabling all peripherals	48MHz	311.25	12.49	329.35	13.28
	HSICLK48, turn off all peripherals	48MHz	311.28	7.39	329.52	7.88
	HSICLK(2), enabling all peripherals	48MHz	162.85	12.17	187.51	14.01
		32MHz	132.34	8.25	154.99	8.83
		24MHz	118.92	6.45	141.01	7.14
		8MHz	64.57	2.39	79.45	2.81
	HSICLK(2), turn off all peripherals	48MHz	162.84	7.41	187.46	7.85
		32MHz	132.32	5.12	154.69	5.86

		24MHz	118.97	4.16	141.07	4.90
		8MHz	64.57	1.61	79.42	1.92

Note: (1) It is tested in comprehensive evaluation instead of in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 43 Program Execution in SRAM, Power Consumption in Running Mode

Parameter	**Condition**	**f_{HCLK}**	**Typical value (1)**		**Maximum value (1)**	
			T_A=25℃，V_{DD}=3.3V		**T_A=105℃，V_{DD}=3.6V**	
			I_{DDA}(μA)	**I_{DD}(mA）**	**I_{DDA}(μA)**	**I_{DD}(mA)**
Power consumption in running mode	HSECLK bypass(2), enabling all peripherals	48MHz	102.37	9.89	119.11	13.45
		32MHz	71.67	6.77	86.72	7.19
		24MHz	58.01	5.19	72.69	5.50
		8MHz	3.48	1.99	12.96	2.28
		1MHz	3.46	0.55	12.79	0.74
	HSECLK bypass(2), turn off all peripherals	48MHz	102.34	5.16	119.22	5.48
		32MHz	71.63	3.61	86.76	3.91
		24MHz	58.00	2.81	72.74	3.11
		8MHz	3.47	1.19	12.76	1.37
		1MHz	3.46	0.45	12.82	0.64
	HSICLK48, enabling all peripherals	48MHz	311.26	10.16	329.53	10.77
	HSICLK48, turn off all peripherals	48MHz	311.29	5.13	329.60	5.53
	HSICLK(2), enabling all peripherals	48MHz	162.85	9.91	187.39	13.37
		32MHz	132.34	6.77	154.96	7.20
		24MHz	118.84	5.20	140.84	5.48
		8MHz	64.57	2.01	79.41	2.23
	HSICLK(2), turn off all peripherals	48MHz	162.83	5.12	187.35	5.49
		32MHz	132.34	3.58	154.77	3.87
		24MHz	118.82	2.79	140.67	3.08
		8MHz	64.57	1.19	79.41	1.38

Notes: (1) It is tested in comprehensive evaluation instead of in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 44 Power Consumption in Sleep mode when the program is executed in SRAM or Flash

Parameter	Condition	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃, V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA）	I_{DDA}(μA)	I_{DD}(mA)
Input the lowest bit	HSECLK bypass(2), enabling all peripherals	48MHz	102.36	6.91	119.16	7.14
		32MHz	71.66	4.67	86.79	4.83
		24MHz	58.04	3.54	72.81	3.71
		8MHz	3.47	1.21	12.91	1.31
		1MHz	3.47	0.17	12.84	0.26
	HSECLK bypass(2), turn off all peripherals	48MHz	102.33	1.49	119.11	1.62
		32MHz	71.64	1.03	86.66	1.15
		24MHz	58.02	0.81	72.65	0.93
		8MHz	3.46	0.29	12.81	0.39
		1MHz	3.46	0.05	12.82	0.16
	HSICLK48, enabling all peripherals	48MHz	311.28	7.08	329.43	7.58
	HSICLK48, turn off all peripherals	48MHz	311.34	1.42	329.48	1.58
	HSICLK(2), enabling all peripherals	48MHz	162.83	6.93	187.55	7.09
		32MHz	132.34	4.68	154.85	4.81
		24MHz	118.84	3.55	140.72	3.67
		8MHz	64.56	1.24	79.47	1.34
	HSICLK(2), turn off all peripherals	48MHz	162.81	1.46	187.36	1.57
		32MHz	132.32	1.01	154.69	1.12
		24MHz	118.81	0.78	140.64	0.88
		8MHz	64.56	0.28	79.39	0.38

Notes: (1) It is tested in comprehensive evaluation instead of in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 45 Power Consumption in Halt and Standby Mode

Parameter	Condition		Typical value(1), (T_A=25℃)						Maximum value(1), (V_{DD}=3.6V)				Unit
			V_{DD}=2.0V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=85℃		T_A=105℃		
			I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	
Power consumption in halt mode	V_{DDA} monitoringON	The voltage regulator is in running mode and all oscillators are off	2.51	20.58	3.70	22.29	4.17	22.98	10.3	62.81	12.09	109.05	μA
		The voltage regulator is in low power mode, and all oscillators are off	2.50	6.57	3.70	8.25	4.16	8.93	10.2	44.14	12.06	88.89	
Power consumption in standby mode		The LSICLK and IWDT are on	2.66	1.86	3.95	3.81	4.42	4.54	10.1	17.81	12.63	30.32	
		The LSICLK and IWDT are off	2.36	1.60	3.45	3.40	3.86	4.09	9.5	17.33	12.09	29.79	
Power consumption in halt mode	V_{DDA} monitoringOFF	The voltage regulator is in running mode and all oscillators are off	1.49	20.55	2.22	22.31	2.56	23.00	8.9	61.25	10.89	109.89	
		The voltage regulator is in low power mode, and all oscillators are off	1.49	6.55	2.21	8.26	2.55	8.93	8.8	42.96	10.79	89.21	
Power consumption in standby mode		The LSICLK and IWDT are on	1.64	1.85	2.46	3.81	2.82	4.54	8.4	17.77	10.99	30.21	
		The LSICLK and IWDT are off	1.34	1.60	1.97	3.40	2.25	4.10	7.8	17.31	10.39	29.75	

Note: It is tested in comprehensive evaluation instead of in production.

Table 46 V_{BAT} Power Consumption

Parameter	Condition	Typical value (1), T_A=25℃				Maximum value (1), V_{BAT}=3.6V				Unit
		V_{BAT}=1.65V	V_{BAT}=1.8V	V_{BAT}=2.4V	V_{BAT}=3.3V	T_A=25℃	T_A=65℃	T_A=85℃	T_A=105℃	
I_{DD_VBAT}	LSECLK and RTC are on, LSECLK oscillator drive capability configuration LSECLKDRV [1:0] =00	0.75	0.80	1.11	1.86	3.35	6.07	9.00	12.18	μA
	LSECLK and RTC are on, LSECLK oscillator drive capability configuration LSECLKDRV [1:0] =11	1.12	1.21	1.61	2.39	4.03	6.72	9.60	12.87	

Note: It is tested in comprehensive evaluation instead of in production.

5.7.3 Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, f_{PCLK}=f_{HCLK}=1M.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 47 Peripheral Power Consumption

Parameter	Peripheral	Typical value (1) T_A=25℃, V_{DD}=3.3V	Unit
Peripheral power consumption	BusMatrix	3.47	μA
	CRC	0.86	
	DMA	4.74	
	FLASH	8.94	
	GPIOA	4.39	
	GPIOB	4.58	
	GPIOC	1.05	
	GPIOD	1.05	
	GPIOE	1.08	
	GPIOF	0.75	
	SRAM	0.47	
	TSC	2.11	
	ALL_AHB	28.95	
	APB_Bridge	1.34	
	ADC	2.66	
	CAN	5.75	
	CEC	0.83	
	CRS	0.66	
	DAC	2.30	
	DBGMCU	0.30	
	I2C1	1.99	
	I2C2	2.22	
	PMU	0.68	
	SPI1	4.27	
	SPI2	4.14	
	SYSCFG	0.93	
	TMR1	7.07	
	TMR2	7.19	

Parameter	Peripheral	Typical value (1) T_A=25℃, V_{DD}=3.3V	Unit
	TMR3	5.47	
	TMR6	1.34	
	TMR7	1.36	
	TMR14	2.65	
	TMR15	4.28	
	TMR16	3.26	
	TMR17	3.43	
	USART1	9.41	
	USART2	9.05	
	USART3	2.77	
	USART4	2.82	
	USBD	48.58	
	WWDT	0.82	
	ALL_APB	127.91	

5.8 Wake-up Time in Low Power Mode

The measurement of wake-up time with low power consumption is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 48 Low Power Wake-up Time

Symbol	Parameter	Condition	Typical value (1), (T_A=25℃)			Maximum value (1)	Unit
			2V	3.3V	3.6V		
$t_{WUSLEEP}$	Wake up from sleep mode	-	4SYSCLK cycles			-	μs
t_{WUSTOP}	Wake up from halt mode	The voltage regulator is in running mode	3.12	2.72	2.65	3.30	
		The voltage regulator is in low power mode	5.63	4.00	3.82	6.15	
$t_{WUSTDBY}$	Wake up from standby mode	-	80.83	38.17	34.74	120.54	

Note: It is tested in comprehensive evaluation instead of in production.

5.9 I/O Port Characteristics

Table 49 DC Characteristics (T_A=-40℃-105℃,V_{DD}=2~3.6V)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IL}	Input low level voltage	STD and STDA I/O	-	-	$0.3V_{DDIOx}$+0.07	V
		5T and 5Tf I/O	-	-	$0.475V_{DDIOx}$ -0.2	
		I/O pins except Boot0	-	-	$0.3V_{DDIOx}$	
V_{IH}	Input high level voltage	STD and STDA I/O	$0.445V_{DDIOx}$ +0.398	-	-	V
		5T and 5Tf I/O	$0.5V_{DDIOx}$ +0.2	-	-	
		I/O pins except Boot0	$0.7V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	STD and STDA I/O	-	200	-	mV
		5T and 5Tf I/O	-	100	-	
I_{lkg}	Input leakage current	STD, 5T and 5Tf I/OTTa in digital mode, VSS≤VIN≤VDDIOx	-	-	+0.1	μA
		STDA in digital mode, V_{DDIOx}≤V_{IN}≤V_{DDA}	-	-	1	
		5T and 5Tf I/O V_{DDIOx}≤V_{IN}≤5V	-	-	10	
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistance	V_{IN}=V_{DDIOx}	25	40	55	kΩ

Table 50 AC Characteristics (T_A =25℃)

SPEED[1:0]	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
10(2MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOX}=2~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output falling time from high to low level		-	120	ns
	$t_{r(IO)out}$	Output rising time from low to high level		-	120	
01(10MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOX}=2~3.6V	-	10	MHz
	$t_{f(IO)out}$	Output falling time from high to low level		-	25	ns
	$t_{r(IO)out}$	Output rising time from low to high level		-	25	
11(50MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=30pF, V_{DD}=2.7~3.6V	-	30	MHz
	$t_{f(IO)out}$	Output falling time from high to low level		-	8	ns
	$t_{r(IO)out}$	Output rising time from low to high level		-	8	
	$f_{max(IO)out}$	Maximum frequency	C_L=50pF，	-	2	MHz

SPEED[1:0]	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
FM+ Configuration	$t_{f(IO)out}$	Output falling time	V_{DDIOx}≥2V	-	11	ns
	$t_{r(IO)out}$	Output rising time		-	33	
FM+ Configuration	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DDIOx}<2V	-	0.5	MHz
	$t_{f(IO)out}$	Output falling time		-	14	ns
	$t_{r(IO)out}$	Output rising time		-	43	

Figure 9 Definition of Input and Output AC characteristics

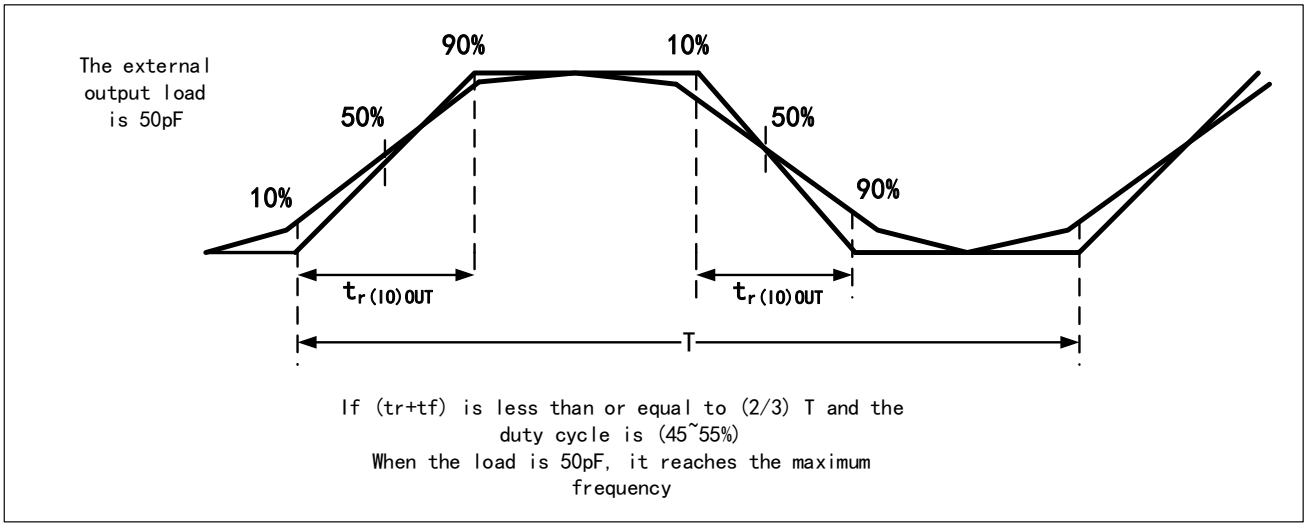


Table 51 Output Drive Current Characteristics (T_A =25℃)

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=8mA, V_{DDIOx}≥2.7V	-	0.4	V
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-0.4	-	
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=20mA, V_{DDIOx}≥2.7V	-	1.3	
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-1.3	-	

Note: It is tested in comprehensive evaluation instead of in production.

5.10 NRST pin characteristics

The input drive of NRST pin adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}

Table 52 NRST Pin Characteristics (T_A=-40~105℃, V_{DD}=2~3.6V)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{IL(NRST)}$	NRST input low voltage	-	-	-	0.3V_{DD}+0.07	V
$V_{IH(NRST)}$	NRST input high voltage	-	0.445V_{DD}+0.398	-	-	

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{hys(NRST)}$	Voltage hysteresis of NRST Schmitt trigger	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	25	40	55	kΩ

5.11 Communication Interface

5.11.1 I2C Interface Characteristics

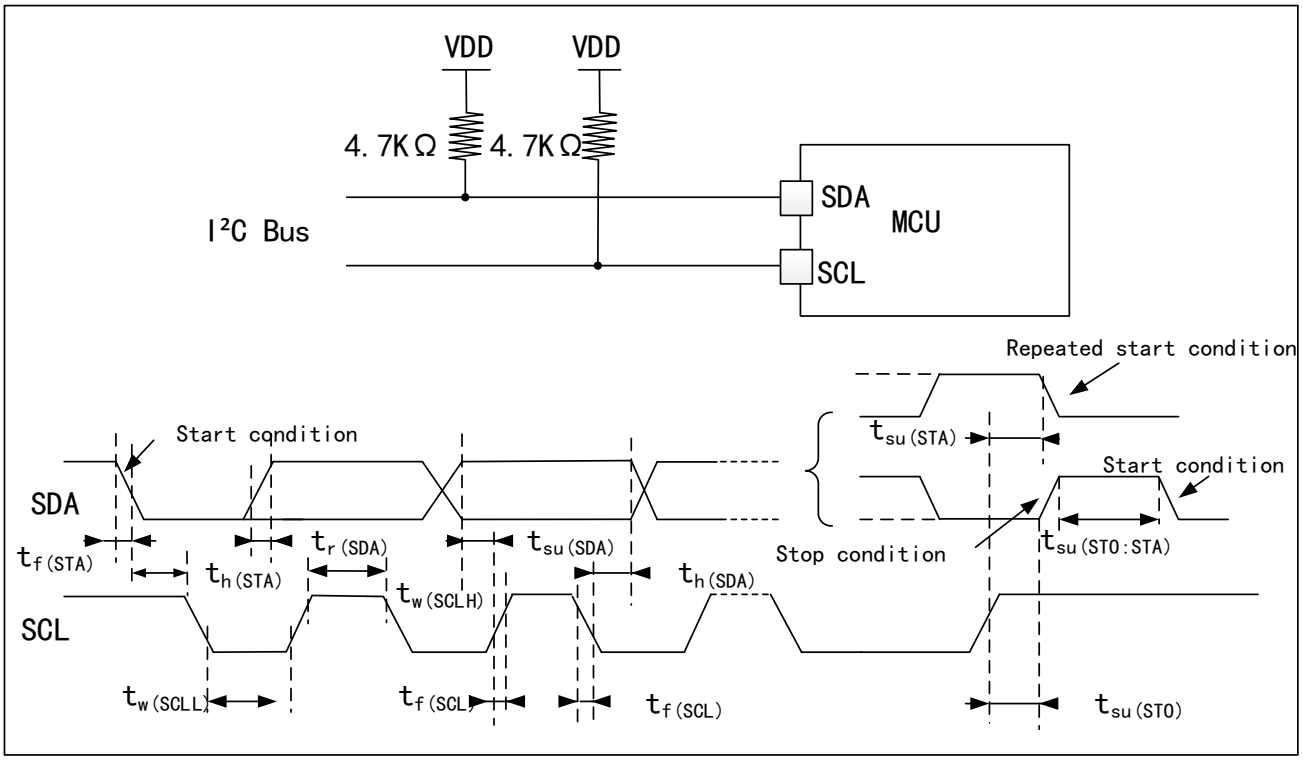
- Standard mode (Sm): Up to 100kbit/s
- Fast mode (Fm): Up to 400kbit/s
- Ultrafast mode (Fm+): Up to 1Mbit/s

Table 53 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Ultrafast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(SCLL)}$	SCL clock low time	4.84	-	1.21	-	0.52	-	μs
$t_{w(SCLH)}$	SCL clock high time	5.09	-	1.14	-	0.46	-	
$t_{su(SDA)}$	SDA setup time	4400	-	860	-	300	-	ns
$t_{h(SDA)}$	SDA data holding time	0	210	0	252	0	145	
$t_{r(SDA)}$/ $t_{r(SCL)}$	SDA and SCL rising time	-	1000	-	300	-	300	
$t_{f(SDA)}$/ $t_{f(SCL)}$	SDA and SCL falling time	-	9.86	-	8.12	-	4	
$t_{h(STA)}$	Start condition holding time	4.96	-	0.68		0.33	-	μs
$t_{su(STA)}$	Repeated start condition setup time	4.9	-	0.87	-	0.54	-	
$t_{su(STO)}$	Setup time of stop condition	4.50	-	1.21	-	0.54	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.67	-	1.37	-	0.77	-	μs

Note: It is tested in comprehensive evaluation instead of in production.

Figure 10 Bus AC Waveform and Measurement Circuit



Note: the measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.11.2 SPI Interface Characteristics

Table 54 SPI Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rising and falling time	Load capacitance: C=15pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4T_{PCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2T_{PCLK}$ + 10	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK}=36MHz, Prescaler coefficient =4	54	57	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	12	-	ns
		Slave mode	20	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	34	-	ns
		Slave mode	22	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK}=20MHz	-	17	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	-	18	ns

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	16	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	6	ns
$t_{h(SO)}$	Data output holding time	Slave mode (after enable edge)	11.5	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	2	-	

Note: It is tested in comprehensive evaluation instead of in production.

Figure 11 SPI Timing Diagram—Slave Mode and CPHA=0

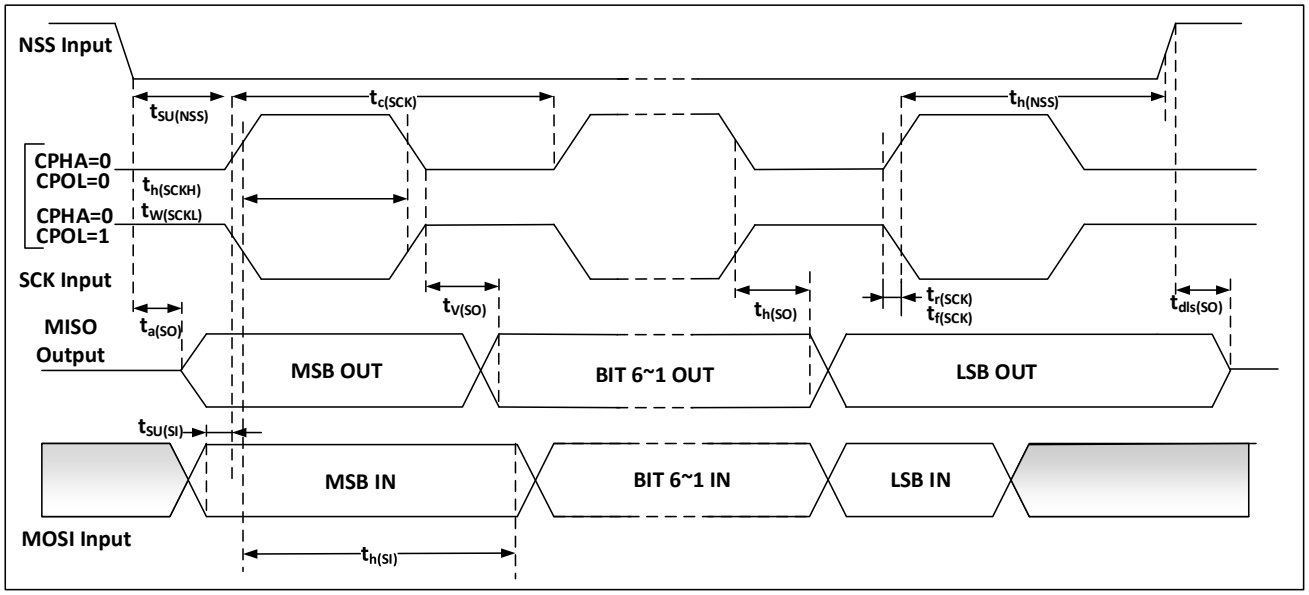
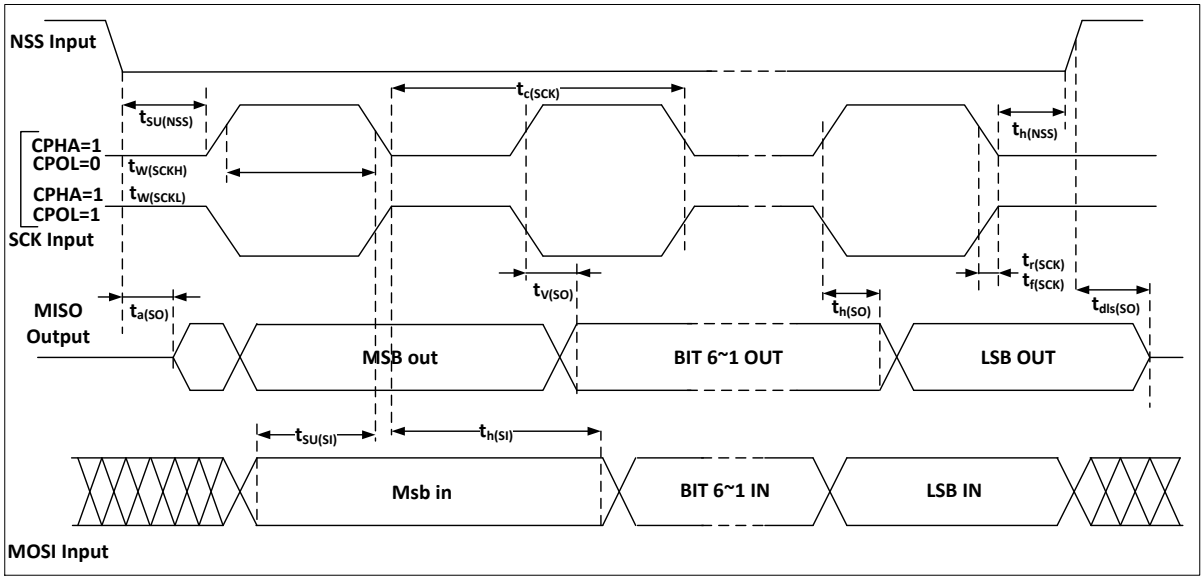
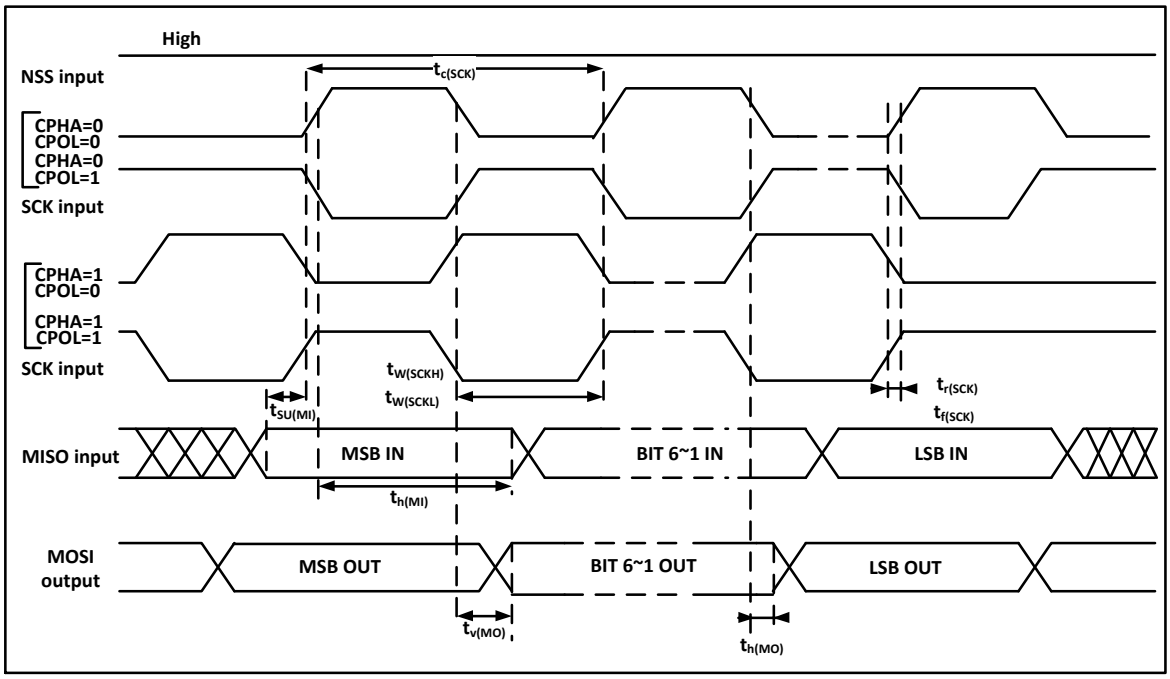


Figure 12 SPI Timing Diagram—slave mode and CPHA=1



Note: the measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 13 SPI Timing Diagram—Master mode



Note: the measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.12 ADC

5.12.1 Built-in Reference Voltage Characteristics

Table 55 Built-in Reference Voltage Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{REFINT}	Built-in reference voltage	-40℃<T_A<+105℃	1.19	1.23	1.27	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10	μs
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	4	-	-	μs
ΔV_{REFINT}	Built-in reference voltage extends to temperature range	V_{DDA}=3.3V	-	-	25	mV

Note: It is tested in comprehensive evaluation instead of in production.

5.12.2 12-bit ADC Characteristics

Table 56 12-bit ADC Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	service voltage	-	2.4	-	3.6	V
I_{DDA}	ADC power consumption	V_{DDA}=3.3V，f_{ADC}=4MHz，Sampling time =1.5 个 f_{ADC}	-	1	-	mA
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sample and hold capacitor	-	-	8	-	pF

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
R_{ADC}	Sampling resistance	-	-	-	1000	Ω
t_S	Sampling time	f_{ADC}=14MHz	0.107	-	17.1	μs
T_{CONV}	Sampling and conversion time	f_{ADC}=14MHz,12-bit conversion	1	-	18	μs

Note: It is tested in comprehensive evaluation instead of in production.

Table 57 Accuracy of 12-bit ADC

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
$\|E_T\|$	Composite error	f_{PCLK}=48MHz, f_{ADC}=14MHz, V_{DDA}=2.4V-3.6V T_A=-40℃~105℃	3.19	4	LSB
$\|E_O\|$	Offset error		1.98	2.7	
$\|E_G\|$	Gain error		3	3.2	
$\|E_D\|$	Differential linear error		0.7	1.4	
$\|E_L\|$	Integral linearity error		1.4	1.6	

Note: It is tested in comprehensive evaluation instead of in production.

5.13 DAC

Test parameter description:

- DNL differential nonlinear error: the deviation between two consecutive codes is——1 LSB
- INL integral nonlinear error: the difference between the measured value at code i and the value at code i on the connection between code 0 and the last code 4095

Table 58 DAC Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
R_{LOAD}	Resistive load	Load is connected to V_{SSA} with buffer on	5	-	-	kΩ
		Load is connected to V_{DDA} with buffer on	-	-	-	
R_O	output impedance	The resistive load between DAC_OUT and V_{SS} is 1.5MΩ with Buffer off	-	-	15	kΩ
C_{LOAD}	Capacitive load	Maximum capacitive load at DAC_OUT pin with buffer on	-	-	50	pF
DAC_OUT	The voltage of DAC_OUT output	The buffer is on, corresponding to 12-bit input codes (0x0E0) to (0xF1C) when V_{DDA}=3.6V and (0x155) and (0xEAB) when V_{DDA}=2.4V	0.2	-	$V_{DDA-0.2}$	V
		The buffer is off, corresponding to the 12-bit input codes (0x0E0) to (0xF1C) when V_{DDA}=3.6V and (0x155) and (0xEAB) when V_{DDA}	-	0.5	$V_{DDA-1LSB}$	mV

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
I_{DDA}	Power consumption of DAC in quiescent mode	Non-load, the input terminal adopts intermediate code (0x800)	-	-	295	uA
		Non-load, input terminal adopts difference code (0xF1C)			340	
DNL	Differential nonlinear error	Configured with 12-bit DAC	-	-	+2	LSB
INL	Integral nonlinear error	Configured with 12-bit DAC	-	-	+4	LSB
Offset	offset error	V_{DDA}=3.6 is configured with12-bit DAC	-	-	+10	LSB
Gain error	Gain error	Configured with12-bit DAC	-	-	+0.4	%

Note: It is tested in comprehensive evaluation instead of in production.

5.14 Comparator

Table 59 Comparator Characteristics

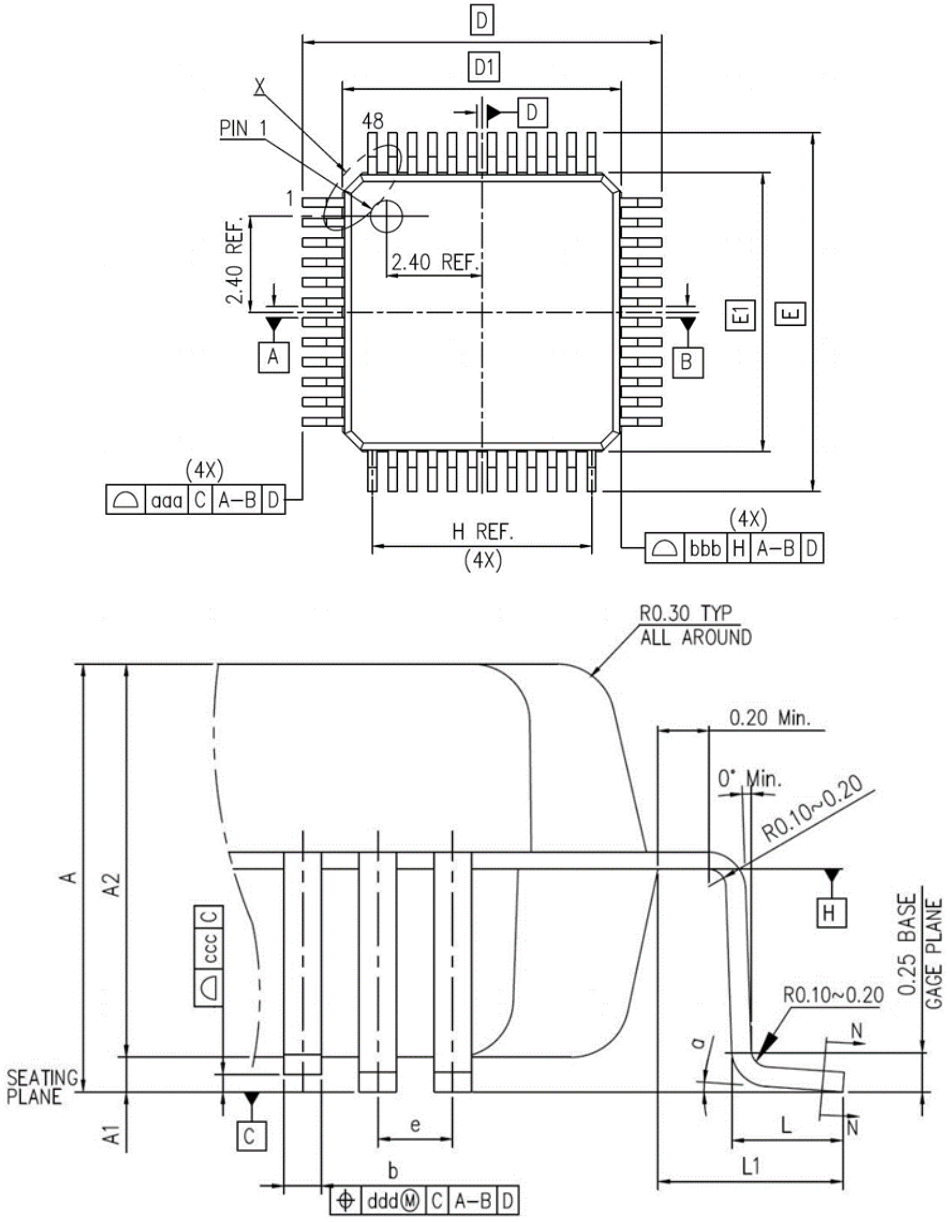
Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Analog supply voltage	-		V_{DD}	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	-
t_D	Full range step, overload propagation delay of 100mV	Very low power mode		-	2	7	μs
		Low power consumption mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		Full speed mode	V_{DDA}≥2.7V	-	90	180	ns
			V_{DDA}＜2.7V	-	110	300	
V_{OFFSET}	offset error	-		-	+4	±10	mv

Note: It is tested in comprehensive evaluation instead of in production.

6 Package Information

6.1 LQFP48 Package Information

Figure 14 LQFP48 Package Diagram



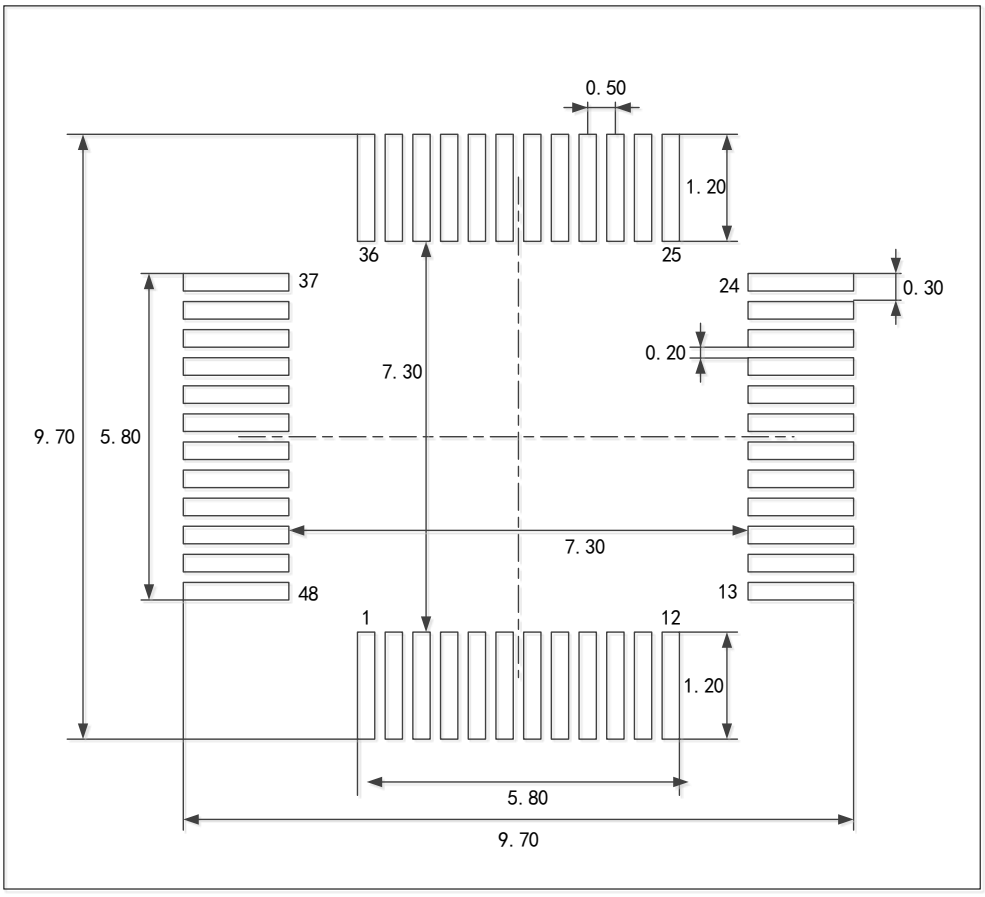
Note: The drawing is not drawn to scale.

Table 60 LQFP48 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.60	OVERALLHEIGHT
2	A2	1.40±0.05	PKGTHICKNESS
3	D	9.00±0.20	LEADTIPTOTIP
4	D1	7.00±0.10	PKGLENGTH
5	E	9.00±0.20	LEADTIPTOTIP
6	E1	7.00±0.10	PKGWIDTH
7	L	0.60±0.15	FOOTLENGTH
8	L1	1.00REF.	LEADLENGTH
9	e	0.50BASE	LEADPITCH
10	H(REF.)	（5.50）	GUM.LEADPITCH
11	b	0.22±0.050	LEADWIDTH

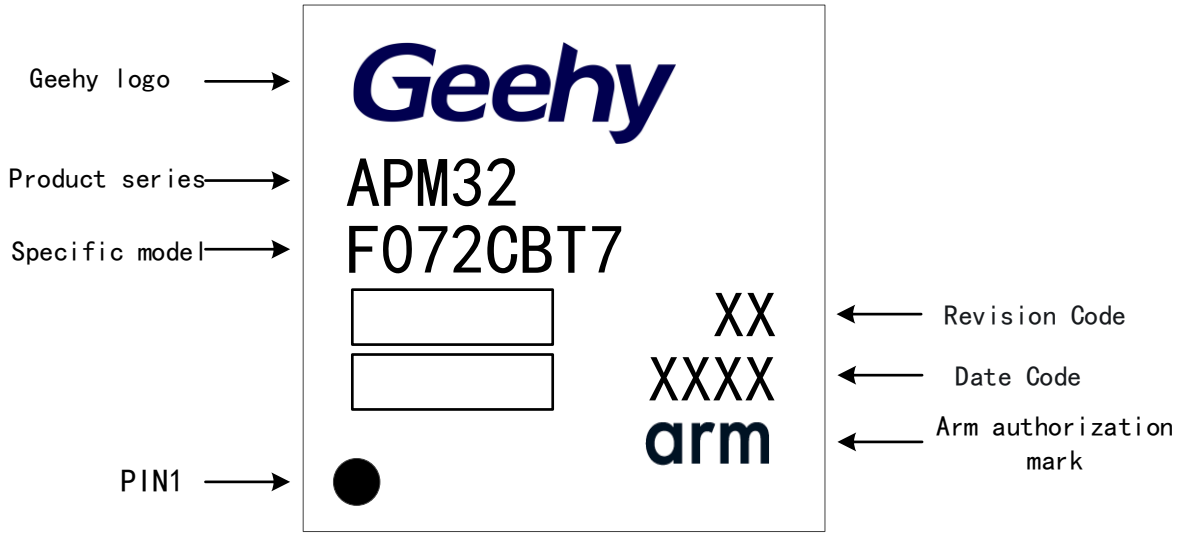
Note: Dimensions are marked in millimeters.

Figure 15 LQFP48 Welding Layout Suggestion



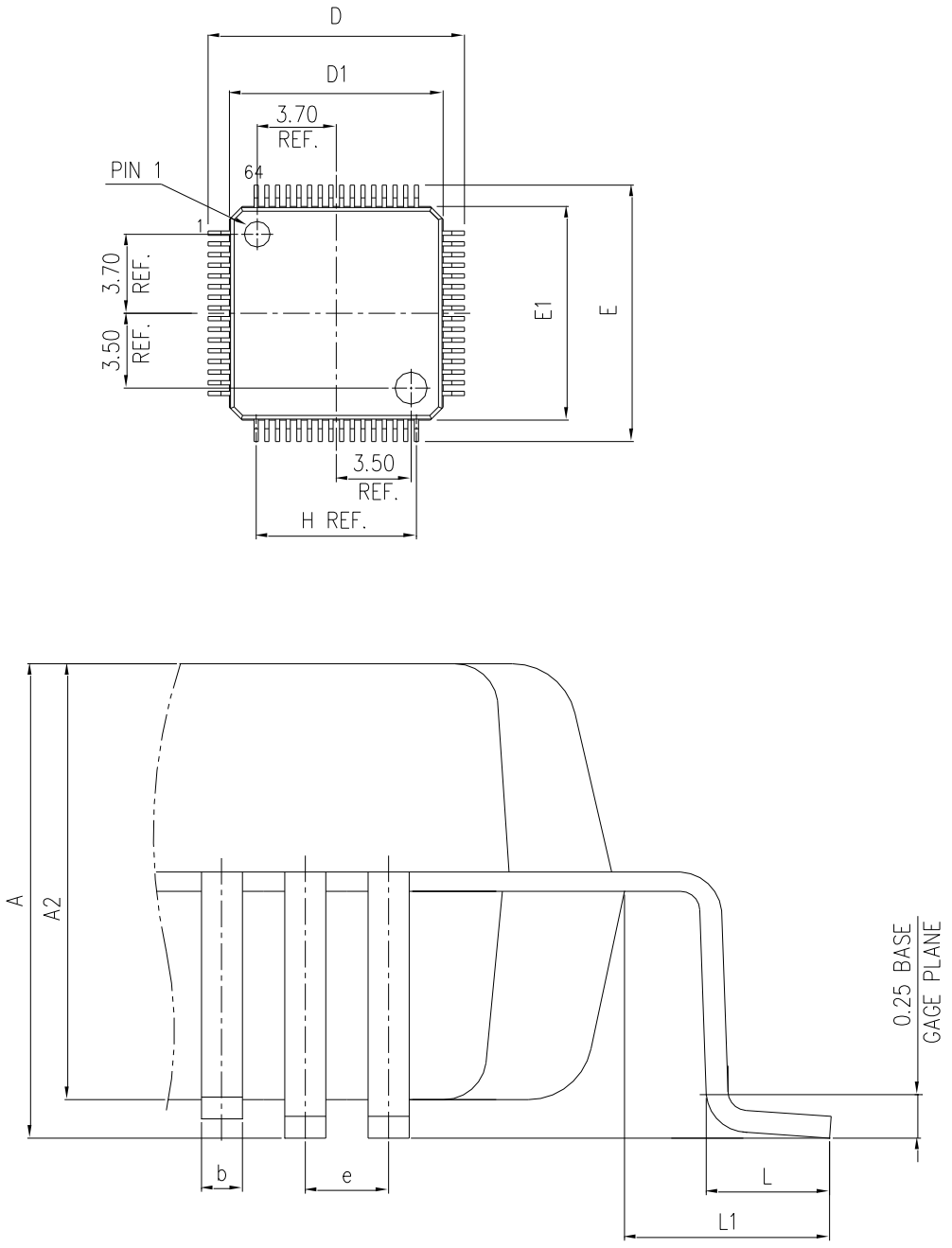
Note: Dimensions are marked in millimeters.

Figure 16 LQFP48 Coding Specification



6.2 LQFP64 Package Information

Figure 17 LQFP64 Package Diagram



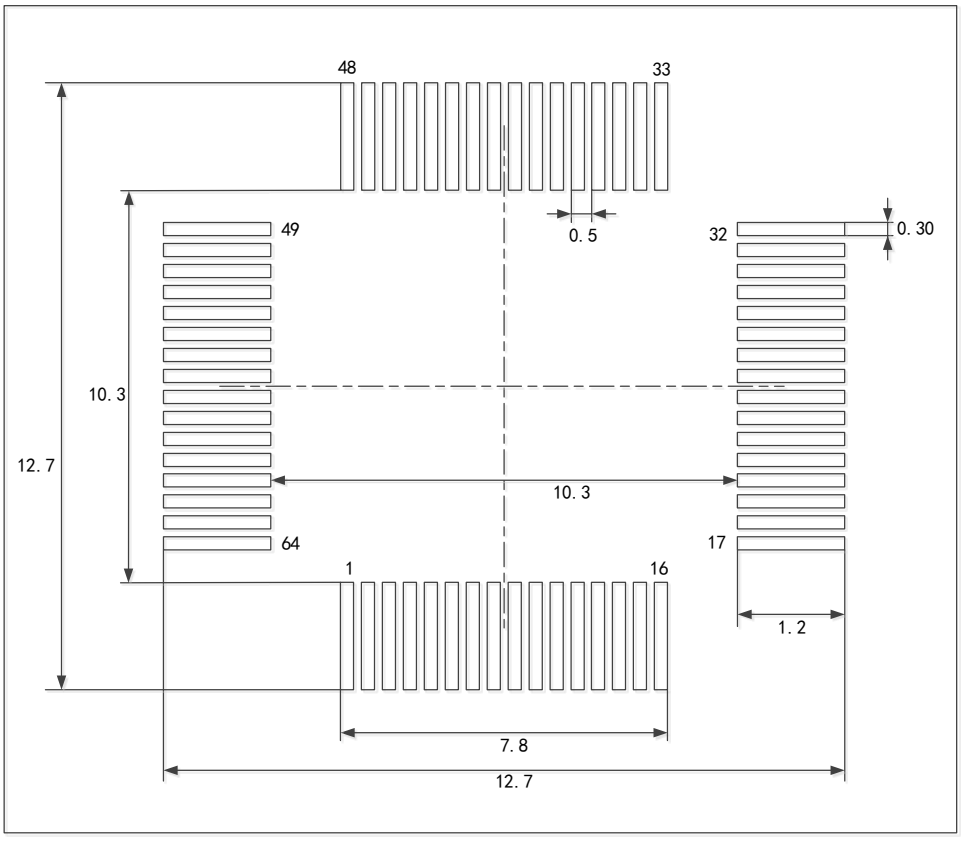
Note: The drawing is not drawn to scale.

Table 61 LQFP64 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.600	OVERALLHEIGHT
2	A2	1.400±0.050	PKGTHICKNESS
3	D	12.000±0.200	LEADTIPTOTIP
4	D1	10.000±0.100	PKGLENGTH
5	E	12.000±0.200	LEADTIPTOTIP
6	E1	10.000±0.100	PKGWIDTH
7	L	0.600±0.150	FOOTLENGTH
8	L1	1.000REF.	LEADLENGTH
9	e	0.500BASE	LEADPITCH
10	H(REF.)	(7.500)	GUM.LEADPITCH
11	b	0.220±0.050	LEADWIDTH

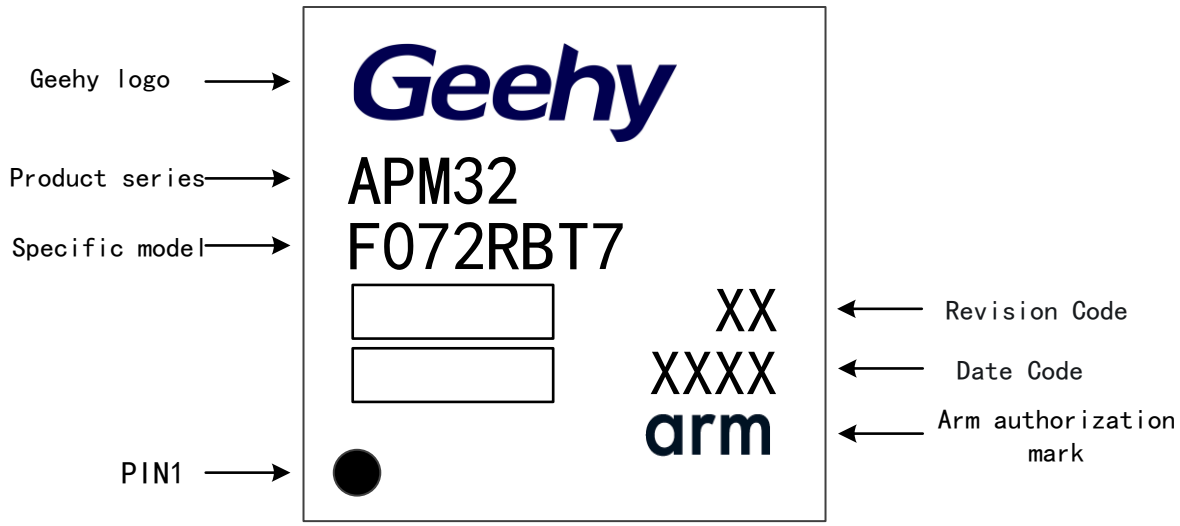
Note: Dimensions are marked in millimeters.

Figure 18 LQFP64 Welding Layout Suggestion



Note: Dimensions are marked in millimeters.

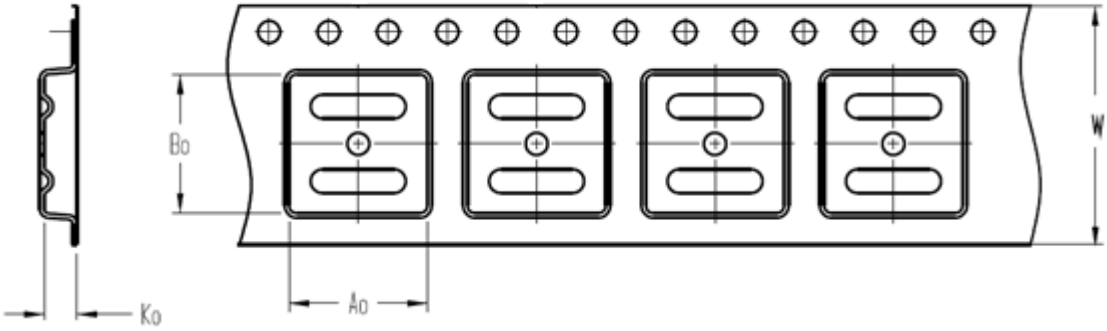
Figure 19 LQFP64 Coding Specification



7 Packaging Information

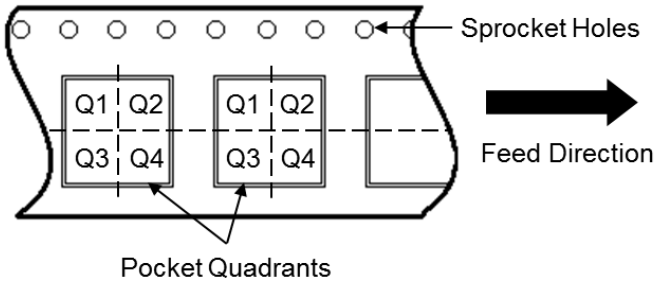
7.1 Reel Packaging

Figure 20 Reel Packaging Specification



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions

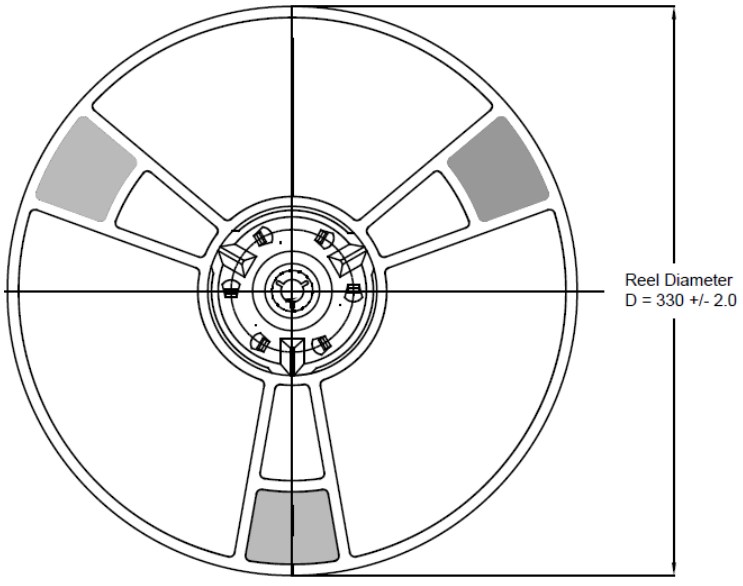
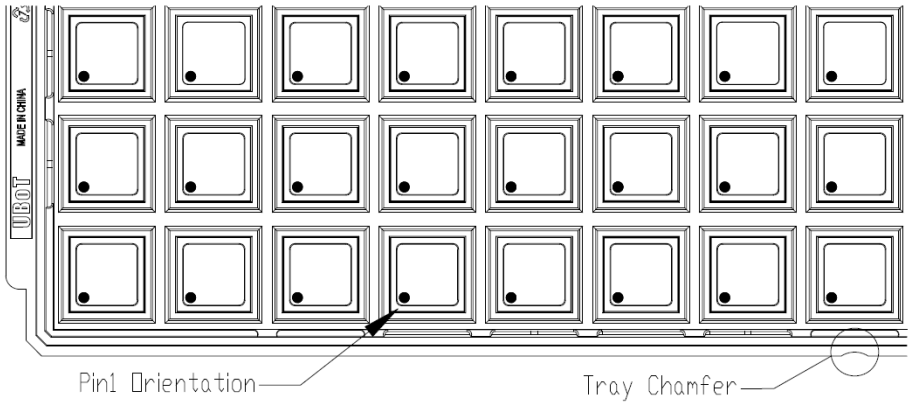


Table 62 Reel Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	ReelDiameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32F072RBT7	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F072CBT7	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1

7.2 Tray Packaging

Figure 21 Tray Packaging Schematic Diagram



Tray Dimensions

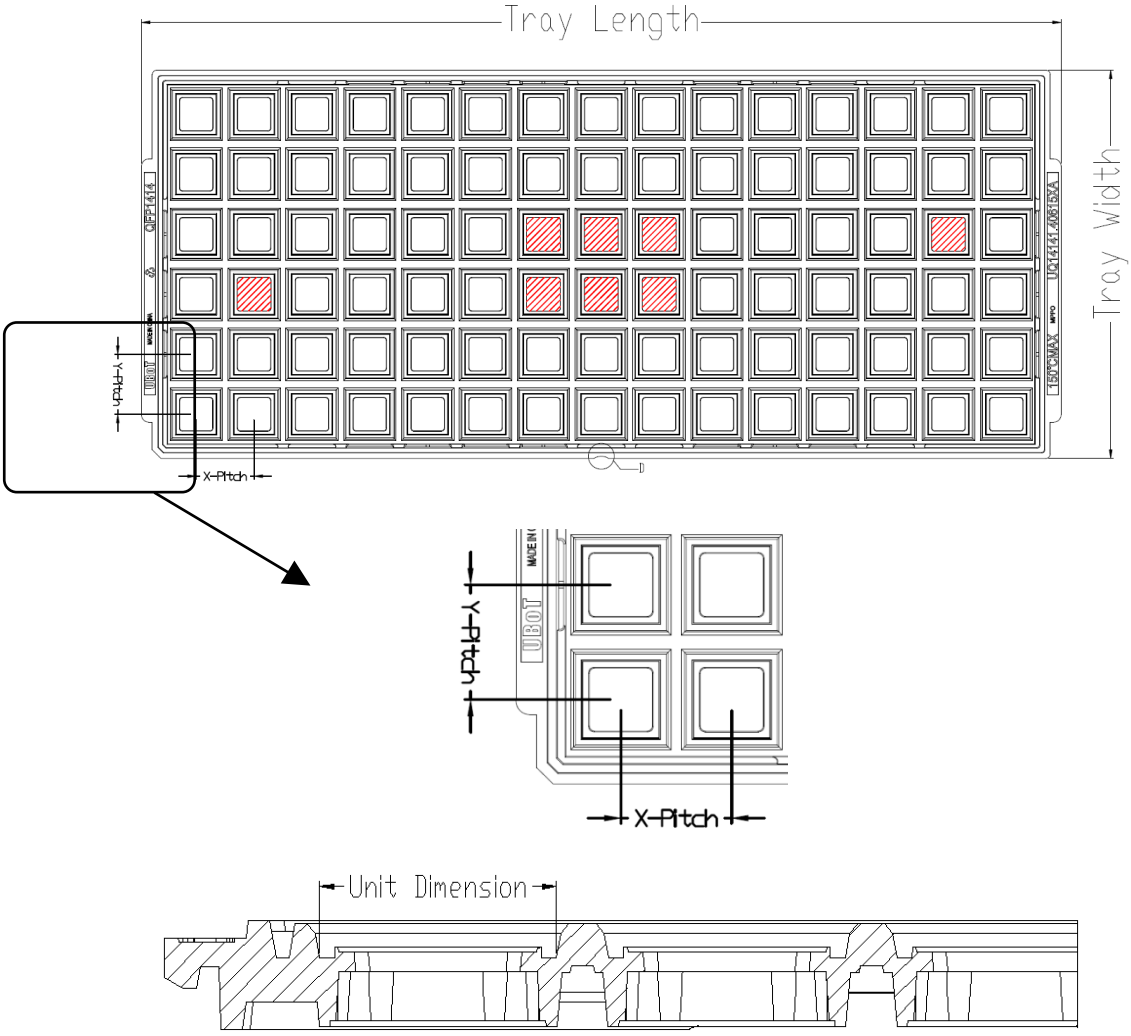


Table 63 Tray Packaging Parameters Specification Table

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-DimensZion (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32F072RBT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F072CBT7	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9

8 Ordering Information

Figure 22 Naming Rules of Ordering Information

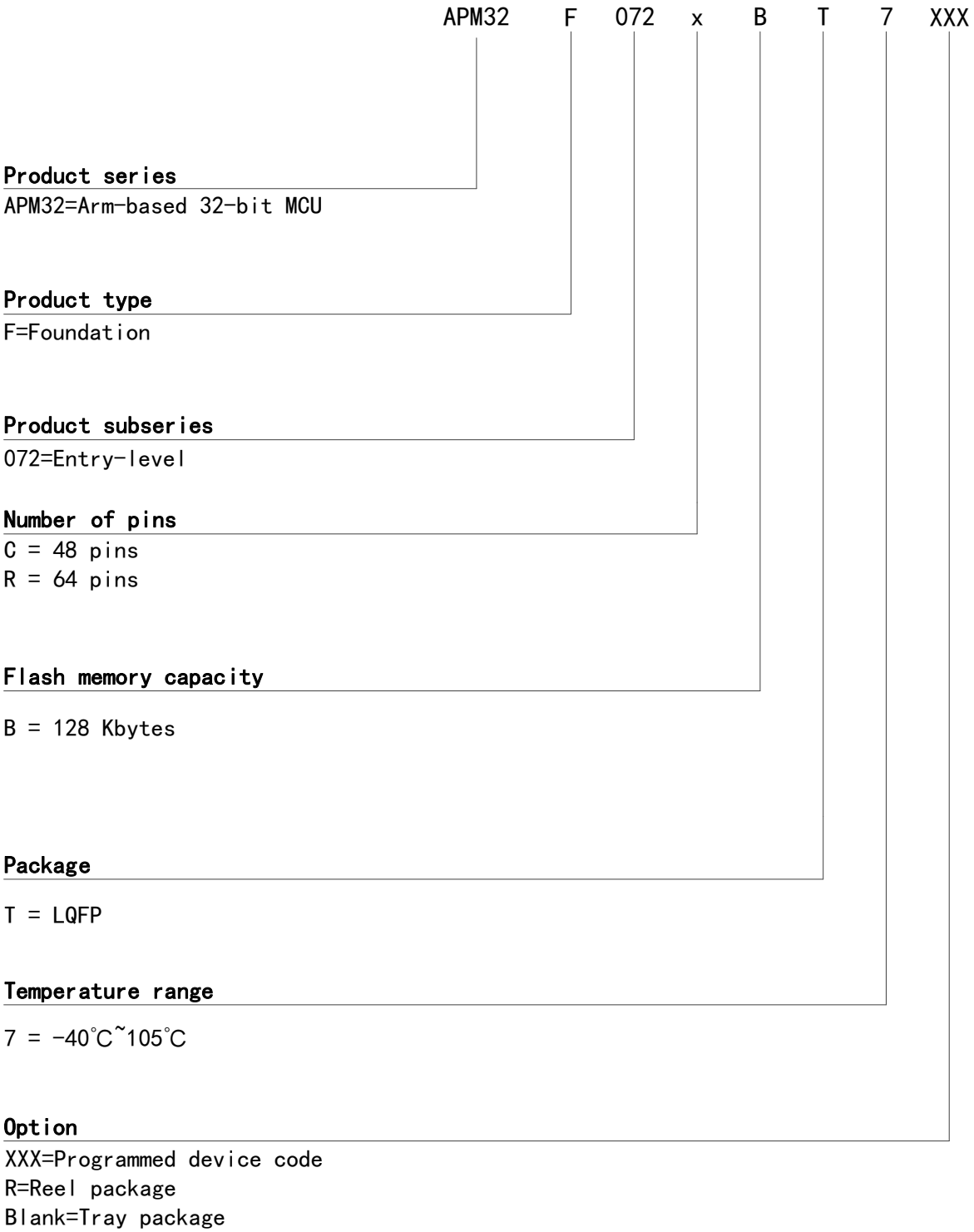


Table 64 List of Ordering Information

Order code	FLASH(KB)	SRAM(KB)	SPQ	Package	Packing	Temperature range
APM32F072RBT7	128	16	1600	LQFP64	Tray	-40℃ ~ 105℃
APM32F072RBT7-R	128	16	1000	LQFP64	Reel	-40℃ ~ 105℃
APM32F072CBT7	128	16	2500	LQFP48	托盘	-40℃ ~ 105℃
APM32F072CBT7-R	128	16	2000	LQFP48	卷带	-40℃ ~ 105℃

Note: SPQ= Smallest Packaging Quantity

9 Naming of Common Functional Modules

Table 65 Naming of Common Function Modules

Full name	简称
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management unit	RCM
External interrupt	EINT
General IO	GPIO
Alternate function IO	AFIO
Wake up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power management unit	PMU
DMA controller	DMA
Attack Damage Carry	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transceiver	UART
Universal asynchronous synchronous transceiver	USART
Flash interface control unit	FMC

10 Revision history

Table 66 Document Revision History

Date	Rivision	Change
May 2022	1.0	New
August 2024	1.1	(1) Modify Product Characteristics (2) Add automotive class description
February 2025	1.2	(1) Add descriptions for APM32F072CBT7
June, 2025	1.3	(1) Add power-on/power-off characteristics

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